# Arijit Raychowdhury

Associate Professor
ON Semiconductor Junior Professor

School of Electrical and Computer Engineering

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## I. Earned Degrees

2002–2007 **Ph.D.**, *Electrical & Computer Engineering*, Purdue University, USA.
1997–2001 **B.E.**, *Electronics & Telecommunication Engineering*, Jadavpur University, India.

## II. Employment

2013-present **Associate Professor**, *School of ECE, Georgia Tech.*, Atlanta, USA.
2010-2013 **Staff Research Scientist**, *Circuit Research, Intel Corporation*, Hillsboro, USA.
2007-2010 **Senior Research Scientist**, *Circuit Research, Intel Corporation*, Hillsboro, USA.
Summer 2006 **Graduate Student Intern**, *Circuit Research, Intel Corporation*, Hillsboro, USA.
Summer 2005 **Graduate Student Intern**, *Circuit Research, Intel Corporation*, Hillsboro, USA.
2002-2007 **Graduate Research & Teaching Assistant**, *Purdue University*, West Lafayette, USA.
2001-2002 **Analog Design Engineer**, *Texas Instruments Inc.*, Bangalore, India.
Summer 2000 **Undergraduate Student Intern**, *Texas Instruments Inc.*, Bangalore, India.

## III. Honors and Awards

### A. International and National Awards

2015 **Early Career Faculty Award**, *Intel Corporation.*
2015 **Best Paper in Analog and Mixed-Signal Track**, *IEEE VLSI-SoC Conference.*
2015 **ON Semiconductor Junior Professorship**, *School of ECE*, Georgia Tech.
2015 **ECE Teaching Fellow**, *School of ECE*, Georgia Tech.
2015 **CISE Research Initiation Initiative (CRII) Award**, *National Science Foundation.*
2014 **Finalist, Qualcomm Innovation Fellowship**, *Team Mentor.*
2014 **Invited Guest & Interviewee**, *KPFT 90.1 Pacifica Radio Houston to discuss the Prospects of Bio-Inspired Computing.*

2014 **Cited in NSF Top News**, *for the paper entitled: Synchronized charge oscillations in correlated electron systems*.

2013 **Honorable Mention**, *The list of Four Decades of Multi-Valued Logic: Lists of Highly Cited Papers*.

2013 **Senior Member**, *IEEE*.

2012 **Best Paper Award**, *International Symposium on Low Power Electronic Design*.

2012 **Divisional Recognition Award**, *For contributions to "Always On" microphones, Intel*.

2011 **Technical Contribution Award**, *Intel*.

2010, 2011 **Patent Recognition Awards**, *Granted for more than seven patents in one year, Intel Corporation*.

2007 **Dimitris N. Chorafas Award**, *presented annually by the Chorafas Foundation (Switzerland) for outstanding doctoral research*.

2007 **Best Thesis Award**, *College of Engineering, Purdue University*.

2006 **Best Paper Award**, *International Symposium on Low Power Electronic Design*.

2005 **Intel Foundation Fellowship**, *Graduate Studies at Purdue University*.

2005 **SRC Technical Excellence Award**, *Research Team Member, Purdue University*.

2003 **Best Paper Award**, *IEEE Nanotechnology Conference*.

2003 **NASA INAC Fellowship**, *NASA Ames Research Center*.

2002 **Meissner Fellowship**, *Purdue University*.

2001 **B. C. Roy Gold Medal**, *First position in the College of Engineering, Jadavpur University among all Engineering Departments*.

2001 **Gold Medal**, *First position in the Department of Electrical & Telecommunication Engineering, Jadavpur University*.

2001 **Winner of Design Award**, *First position in the World DSP Meet, Texas Instruments for the paper entitled, Extended Kalman filter based target tracking in mobile robots using TMS320C2x*.

1997 **Governor's Gold Medal**, *First position in the School Leaving Examination, Std 12, in the state among 500,000+ students*.

# IV. Research, Scholarship, and Creative Activities

## A. Published Books, Book Chapters, and Edited Volumes

Note: **Boldface** font is used to identify co-authors who were students being advised by Prof. Raychowdhury

### A1. Books

No data

### A2. Refereed Book Chapters

BC1. Arijit Raychowdhury and Kaushik Roy, "Nanometer Scale Technologies: Device Considerations" in *"Nano, Quantum and Molecular Computing: Implications To High Level Design And Validation"*, Kluwer Academic Publishers, ISBN: 1402080670, June 2004.

BC2. Ali Keshavarzi and Arijit Raychowdhury, "Carbon nanotubes for digital circuits: Promises, Challenges and Outlook" in *"Carbon Nanotube Electronics (Series on Integrated Circuits and Systems)"*, ISBN-10:

0387368337 August 2008.

BC3. Amit Agarwal, Saibal Mukhopadhyay, Chris H. Kim, Arijit Raychowdhury and Kaushik Roy, "Power Estimation and Reduction" in *"System on Chip: Next Generation Electronics"*, IEE Press, ISBN: 0-86341-552-0, 2009.

BC4. Bipul Paul and Arijit Raychowdhury, "Digital Subthreshold for Ultra-Low Power Operation: Prospects and Challenges," in *"Low-Power Variation-Tolerant Design in Nanometer Silicon"*, Springer Publications, USA, October 2010.

BC5. **Anvesha Amravati**, **Manan Chung** and Arijit Raychowdhury, "A SAR Pipeline ADC with Time Interleaved DAC Sharing for Ultra-Low Power Camera Front Ends," in *"VLSI-SoC: From Systems to Chips"*, Springer Publications, USA, 2016.

### A3. Edited Volumes

No data

## B. Refereed Publications and Submitted Articles

### B.1. Published and Accepted Journal Articles

J1. A. Raychowdhury, B. Gupta, and R. Bhattacharjee, " Bandwidth improvement of microstrip antennas through a genetic-algorithm-based design of a feed network," *Microwave and Optical Technology Letters*, Vol. 27, Issue 4, 2000, pp: 273-275.

J2. I. Saha Misra, A. Raychowdhury, K. K. Mallik, and M. N. Roy. "Design and optimization of a non-planar multidipole array using genetic algorithms for mobile communications," *Microwave and Optical Technology Letters*, Vol. 32, Issue 4, 2002, pp:301-304.

J3. Arijit Raychowdhury, Saibal Mukhopadhyay and Kaushik Roy, "A Circuit Compatible Model of Ballistic Carbon Nanotube Field Effect Transistors", *IEEE Transactions on Computer Aided Design (TCAD)*, Vol. 23, no. 10, Oct. 2004, pp: 1411-1420. (**Most downloaded paper of 2004**)

J4. B. C. Paul, A. Raychowdhury, and K. Roy, "Device Optimization for Digital Subthreshold Operation," *IEEE Transactions on Electron Devices (TED)*, Vol. 52, Issue 2, Feb. 2005 pp: 237- 247.

J5. Arijit Raychowdhury and Kaushik Roy, "Carbon nanotube based voltage-mode multiple-valued logic design," *IEEE Transactions on Nanotechnology (TNANO)*, Vol. 4, Issue 2, Mar. 2005, pp: 168-179 (**Featured in Forty Years of Multi-Valued Logic**).

J6. Saibal Mukhopadhyay, Arijit Raychowdhury and Kaushik Roy, "Accurate Estimation of Total Leakage in Nanometer Scale Bulk CMOS Circuits Based on Device Geometry and Doping Profile," *IEEE Transactions on Computer Aided Design (TCAD)*, Vol. 24, Issue 3, Mar. 2005, pp: 363-381.

J7. Swarup Bhunia, Arijit Raychowdhury and Kaushik Roy, "Frequency Specification Testing of Analog Filters Using Wavelet Transform of Dynamic Supply Current," *Journal of Electronic Testing: Theory and Applications*, March 2005.

J8. Swarup Bhunia, Arijit Raychowdhury and Kaushik Roy, "Defect Oriented Testing of Analog Circuits Using Wavelet Analysis of Dynamic Supply Current," *Journal of Electronic Testing: Theory and Applications*, Vol. 21, Issue 2, April 2005.

J9. Myeong-Eun Hwang, Arijit Raychowdhury, and Kaushik Roy, "Energy Recovery Techniques to Reduce On-chip Power Density in Molecular Nano-Technologies", *IEEE Transactions on Circuits and Systems I (TCAS-I)*, Vol. 52, no. 8, Aug. 2005, pp: 1580-1589.

J10. Arijit Raychowdhury, Bipul Paul, Swarup Bhunia, and Kaushik Roy, "Computing with Subthreshold Leakage: Device/Circuit/Architecture Co-design for Ultralow-Power Subthreshold Operation", *IEEE Transactions on Very Large Scale Integration Systems (TVLSI)*, Vol. 13, Issue 11, Nov. 2005, pp: 1213-1224.

J11. Arijit Raychowdhury and Kaushik Roy, "Modeling of Metallic Carbon Nanotube Interconnects for Circuit Simulations and a Comparison with Cu Interconnects for Scaled Technologies", *IEEE Transactions on Computer Aided Design (TCAD)*, Vol. 25, Issue 1, Jan. 2006, pp: 58-65.

J12. N. Banerjee, A. Raychowdhury, K. Roy, S. Bhunia, and H. Mahmoodi, "Novel Low-Overhead Operand Isolation Techniques for Low-Power Datapath Synthesis" , *IEEE Transactions on Very Large Scale Integration Systems (TVLSI)*, Vol. 14, Issue 9, Sep. 2006, pp: 1034-1039.

J13. Arijit Raychowdhury, Ali Keshavarzi, Juanita Kurtin, Vivek De, and Kaushik Roy, "Analysis of Carbon Nanotube Field Effect Transistors for High Performance Digital Logic - Modeling and DC Simulations", *IEEE Transactions on Electron Devices (TED)*, Vol. 53, Issue 11, Nov. 2006, pp: 2711-2717.

J14. Ali Keshavarzi, Arijit Raychowdhury, Juanita Kurtin, Kaushik Roy, and Vivek De, "Analysis of Carbon Nanotube Field Effect Transistors for High Performance Digital Logic Transient Analysis, Parasitics and Scalability", *IEEE Transactions on Electron Devices (TED)*, Vol. 53, Issue 11, Nov. 2006, pp: 2718-2726.

J15. Swaroop Ghosh, Swarup Bhunia, Arijit Raychowdhury and Kaushik Roy, "A Novel Delay Fault Testing Methodology Using Low-Overhead Built-in Delay Sensor," *IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems (TCAD)*, Vol 25, Issue 12, Dec. 2006, pp: 2934-2943.

J16. Arijit Raychowdhury, and Kaushik Roy, "Carbon Nanotube Electronics: Design of High Performance and Low Power Digital Circuits", *IEEE Transactions on Circuits and Systems (TCAS) I*, Vol. 54, Issue 11, Nov. 2007, pp 2391-2401.

J17. A. Coker, V. Taylor, D. Bhaduri, S. Sukla, A. Raychowdhury, K. Roy, "Multi-junction Fault Tolerance Architecture for Nanoscaled Crossbar memory," *IEEE Transactions on Nanotechnology (TNANO)*, Vol. 7, Issue 2, Mar. 2008, pp: 202-208.

J18. Arijit Raychowdhury, Shekhar Borkar, Vivek De, Ali Keshavarzi and K. Roy, "Variation Tolerance in a Multi-channel Carbon Nanotube Transistor for High Speed Digital Circuits," *IEEE Transactions on Electron Devices (TED)*, Vol 56, Issue 3, Mar. 2009, pp: 383-392.

J19. Sumeet Kumar Gupta, Arijit Raychowdhury and K. Roy, "Compact models considering incomplete voltage swing in complementary metal oxide semiconductor circuits at ultralow voltages: A circuit perspective on limits of switching energy," *Journal of Applied Physics (JAP)*, Vol. 105, Issue 9, May 2009.

J20. Y. William Li, Hasnain Lakdawala, Arijit Raychowdhury, Greg Taylor, K. Soumyanath, "A 1.05V 1.6mW, 0.45°C $3\sigma$ Resolution $\Sigma\Delta$ based Temperature Sensor with Parasitic Resistance Compensation in 32nm Digital CMOS Process," *Journal of Solid State Circuits (JSSCC)*, Vol 44, Issue 12, Dec. 2009, pp: 3621-3630.

J21. Sumeet Kumar Gupta, Arijit Raychowdhury and K. Roy, "Digital Computation in Sub-Threshold Region for Ultra-Low Power Operation: A Device-Circuit-System Co-Design Perspective," *Proceedings of IEEE*, Vol. 98, Issue 2, Feb. 2010

J22. Keith A. Bowman, James W. Tschanz, Shih-Lien L. Lu, Paolo A. Aseron, Muhammad M. Khellah, Arijit Raychowdhury, Bibiche M. Geuskens, Carlos Tokunaga, Chris B. Wilkerson, Tanay Karnik, and Vivek K. De, "A 45nm Resilient Microprocessor Core for Dynamic Variation Tolerance," *Journal of Solid State Circuits (JSSC)*, Issue 12, Dec. 2010, pp: 282 - 283.

J23. Arijit Raychowdhury, Bibiche Geuskens, Keith Bowman, James Tschanz, Shih-Lien Lu, Tanay Karnik, Muhammad Khellah, Vivek De, "Tunable Replica Bits for Dynamic Variation Tolerance in 8T SRAM Arrays," *Journal of Solid State Circuits (JSSC)*, Vol. 46, Issue 4, Apr. 2011, pp: 797-805.

J24. Bowman, K.A., Tokunaga, C., Tschanz, J.W., Raychowdhury, A., Khellah, M.M., Geuskens, B.M., Lu, S.-L.L, Aseron, P.A., Karnik, T., De, V.K. , "All-Digital Circuit-Level Dynamic Variation Monitor for Silicon Debug and Adaptive Clock Control," *IEEE Transactions on Circuits and Systems (TCAS) I: Regular Papers* , Vol. 58, no.9, Sep. 2011, pp: 2017-2025.

J25. C. Augustine, A. Raychowdhury, D. Somasekhar, K. Roy, V. De, "Design Space Exploration of Typical STT MTJ Stacks in Memory Arrays in the Presence of Variability and Disturbances," *Transactions on Electron Devices (TED)*, Vol. 58, Issue 12, Dec. 2011.

J26. Arijit Raychowdhury, Carlos Tokunaga, Willem Beltman, Michael Deisher, James Tschanz, Vivek De, "A 2.3nJ/Frame Voice Activity Detector for Context-Aware Systems in 32nm CMOS," *Journal of Solid State Circuits (JSSC)*, Mar. 2013.

J27. Helia Naeimi, Charles Augustine, Arijit Raychowdhury, Shih-Lien Lu, James Tschanz,"STTRAM Scaling and Retention Failure," *Intel Technology Journal (ITJ)*, May 2013.

J28. Nikhil Shukla, **Abhinav Parihar**, Eugene Freeman, Hanjong Paik, Greg Stone, Vijaykrishnan Narayanan, Haidan Wen, Zhonghou Cai, Venkatraman Gopalan, Roman Engel-Herbert, Arijit Raychowdhury, Suman Datta, "Synchronized charge oscillations in correlated electron systems," *Nature Scientific reports (SR)*, Vol. 4, April 2014.

J29. **Samantak Gangopadhyay**, Dinesh Somasekhar, James Tschanz, Vivek De, Arijit Raychowdhury, "A 32nm Embedded, Fully-Digital, Phase-Locked Low Dropout Regulator for Fine Grained Power Management in Digital Circuits", *Journal of Solid State Circuits (JSSC)*, Vol. 11, Nov. 2014.

J30. **Abhinav Parihar**, Nikhil Shukla, Suman Datta, Arijit Raychowdhury, "Exploiting Synchronization Properties of Correlated Electron Devices in a Non-Boolean Computing Fabric for Template Matching," *IEEE Journal On Emerging And Selected Topics In Circuits And Systems(JETCAS)*, Vol. 4, Dec. 2014.

J31. **Abhinav Parihar**, Nikhil Shukla, Suman Datta, Arijit Raychowdhury, "Synchronization of pairwise-coupled, identical, relaxation oscillators based on metal-insulator phase transition devices: A model study," *Journal of Applied Physics (JAP)*, Feb. 2015.

J32. P. Maffezzoni, L. Daniel, **N. Shukla**, S. Datta, A. Raychowdhury, V. Narayanan, "Modelling hysteresis in vanadium dioxide oscillators," *Electronic Letters*, Vol. 51, Issue 11, 28 May 2015, p. 819-820

J33. Paolo Maffezzoni, Luca Daniel, **N. Shukla**, Suman Datta, Arijit Raychowdhury, "Modeling and Simulation of Vanadium dioxide Relaxation Oscillators," *IEEE Transactions on Circuits and System (TCAS) I: Regular Papers*, Vol.62, Issue 9, pp.2207-2215, Sept. 2015.

J34. **Soham Desai**, M. Shoaib and A. Raychowdhury, "An Ultra-low power, "Always-On" Camera Front-End for Posture Detection in Body Worn Cameras using Restricted Boltzman Machines," *IEEE Transactions on Multi-Scale Computing Systems (TMSCS)*, Vol. 1, Issue 4, pp: 187 - 194, Dec. 2015.

J35. **Ashwin Chintaluri**, S. Natarajan, Helia Naeimi and A. Raychowdhury, "Analysis of Defects and Fault models in Embedded Spin Transfer Torque (STT) MRAM Arrays," *IEEE Journal On Emerging And Selected Topics In Circuits And Systems(JETCAS)*, vol. PP, no. 99, pp. 111, 2016.

J36. R. Venkatesan, V. Kozhikkottu, M. Sharad, C. Augustine, A. Raychowdhury, K. Roy, A. Raghunathan, "Cache Design with Domain Wall Memories," *IEEE Transactions in Computers*, Vol. 65, Issue 4, pp: 1010-1024, 2016.

J37. Wei-Yu Tsai, X. Li, M. Jerry, B. Xie, N. Shukla, H. Liu, N. Chandramoorthy, M. Cotter, A. Raychowdhury, D. Chiarulli, S. Levitan, S. Datta, J. Sampson, N. Ranganathan, V. Narayanan, "Enabling New Computation Paradigms with HyperFET - an Emerging Device," in *IEEE Transactions on Multi-Scale Computing Systems*, Vol. 2, Issue 1, pp: 30-48, 2016.

J38. **Saad Bin Nasir**, and A. Raychowdhury, "All-digital low-dropout regulator with adaptive control and reduced dynamic stability for digital load circuits," *IEEE Transactions on Power Electronics (TPE)*, to appear.

J39. Sandip Roy, Yier Jin and A. Raychowdhury, "The Changing Computing Paradigm with Internet of Things: A Tutorial Introduction," *IEEE Design and Test Magazine (IEEE D&T)*, Vol. 33, Issue 2, pp: 76-96, 2016.

### B.2. Conference Publications with Proceedings (Refereed)

C1. Saibal Mukhopadhyay, Arijit Raychowdhury, and Kaushik Roy, "Accurate Estimation of Total Leakage Current in Scaled CMOS Logic Circuits Based on Compact Current Modeling", Proceedings of the *Design Automation Conference (DAC)*, Anaheim, Jun. 2003, pp. 169-174 (**Nominated for best paper award**).

C2. Arijit Raychowdhury and Kaushik Roy, "Performance Estimation in Molecular Crossbar Architecture Considering Capacitive and Inductive Coupling Between Interconnects", Proceedings of the *IEEE-Nano Conference*, San Francisco, Aug. 2003, pp: 445-448.

C3. Arijit Raychowdhury, Saibal Mukhopadhyay, and Kaushik Roy, "Circuit-compatible modeling of carbon nanotube FETs in the ballistic limit of performance", Proceedings of the *IEEE-Nano Conference*, San Francisco, Aug. 2003, pp: 343-346 (**Best paper award**).

C4. Arijit Raychowdhury, Saibal Mukhopadhyay, and Kaushik Roy, "Modeling of Ballistic Carbon Nanotube Field Effect Transistors for Efficient Circuit Simulation", Proceedings of the *International Conference on Computer Aided Design (ICCAD)*, San Jose, Nov. 2003, pp: 465-469.

C5. S. Oswal, F. Mujica, S. Prasad, R. Srinivasa, B. Sharma, A. Raychowdhury, H. Khasnis, A. Sharma, R. Sriram, B. Vijayvardhan, R. Menon, R. Gireesh, N. Ahuja, M. Gambhir, M. Sadafale, "A 0.13m CMOS Four-channel ADSL2+ Analog Front-end for CO Applications with 75mW per Channel," Digest of Technical Papers of the *International Solid-State Circuits Conference (ISSCC)* Vol.1, Feb. 2004, pp: 404 - 535 .

C6. Arijit Raychowdhury and Kaushik Roy, "A Novel Multiple-Valued Logic Design Using Ballistic Carbon nanotube FETs", Proceedings of the *34th International Symposium on Multiple-Valued Logic (ISMVL)*, Toronto, May 2004, pp: 14-19 (**Featured in Forty Years of Multi-Valued Logic**).

C7. Arijit Raychowdhury, Jing Guo, Kaushik Roy, and Mark Lundstrom, "Choice of Flat-Band Voltage, VDD and Diameter of Ambipolar Schottky-Barrier Carbon Nanotube Transistors in Digital Circuit Design", Proceedings of the *Fourth IEEE Nano Conference*, Munich, Aug. 2004, TH-2-2-1.

C8. Bipul C. Paul, Arijit Raychowdhury, and Kaushik Roy, "Device Optimization for Ultra-Low Power Digital Sub-Threshold Operation", Proceedings of the *International Symposium on Low Power Electronics and Design (ISLPED)*, Newport Beach, USA, Aug. 2004, pp: 96-101.

C9. Arijit Raychowdhury and Kaushik Roy, "Modeling and Analysis of Carbon Nanotube Interconnects for High Speed VLSI Design", Proceedings of the *Fourth IEEE Nano Conference*, Munich, Aug. 2004, WE-P-37.

C10. Arijit Raychowdhury and Kaushik Roy, "Carbon Nanotubes as Interconnects of the Future: A Circuit Perspective", Proceedings of the *Advanced Metallization Conference*, San Diego, Oct. 2004.

C11. Arijit Raychowdhury and Kaushik Roy, "Circuit Modeling of Carbon Nanotube Interconnects and their Performance Estimation in VLSI Design", Proceedings of the *International Workshop on Computational Electronics (IWCE)*, West Lafayette, Oct. 2004.

C12. S. Bhunia, H. Mahmoodi, A. Raychowdhury, K. Roy, "First Level Hold: A Novel Low-overhead Delay Fault Testing Technique," Proceedings of the *International Symposium on Defect and Fault Tolerance in VLSI Systems (DFT)*, Oct. 2004.

C13. Arijit Raychowdhury and Kaushik Roy, "A Circuit Model for Carbon Nanotube Interconnects: Comparative Study with Cu Interconnects for Scaled Technologies", Proceedings of the *International Conference on Computer Aided Design (ICCAD)*, San Jose, Nov. 2004, pp: 237-240.

C14. A. Raychowdhury, and Kaushik Roy, "Carbon Nanotubes for Digital Circuit Design", Proceedings of the *Government Microcircuit Applications and Critical Technology Conference*, GomacTech, Mar. 2005.

C15. A. Raychowdhury, S. Ghosh, S. Bhunia, K. Roy, "A Novel Delay Fault Testing Methodology using On-Chip Low-overhead Delay Measurement Hardware at Strategic probe Points," Proceedings of the *European Testing Symposium (ETS)*, May 2005, pp: 108-113.

C16. A. Raychowdhury, S. Ghosh, K. Roy, "A Novel On-Chip Delay Measurement Hardware for Efficient Speed Binning," Proceedings of the *International On-Line Testing Symposium (IOLTS)*, Jul. 2005, pp: 287-292.

C17. Arijit Raychowdhury, Jing Guo, Kaushik Roy, and Mark Lundstrom, "Design of a novel three-valued static memory using Schottky barrier carbon nanotube FETs", Proceedings of the *Fourth IEEE Nano Conference*, Munich, Jul. 2005, pp: 507 510.

C18. A. Raychowdhury, S. Mukhopadhyay, and K. Roy, "A Feasibility Study of Subthreshold SRAM across Technology Generations", Proceedings Of the *International Conference on Computer Design (ICCD)*, San Jose, Aug. 2005, pp: 417-422.

C19. S. Mukhopadhay, A. Raychowdhury, K. Roy, H. Mahmoodi, "Leakage Current Based Stabilization Scheme for Robust Sense Amplifier Design for Yield Enhancement in Nanoscale SRAM," Proceedings of the *Asian Test Symposium (ATS)*, Dec. 2005, pp: 176-181.

C20. A. Raychowdhury, Bipul Paul, Swarup Bhunia, and Kaushik Roy, "Ultralow Power Computing with Subthreshold Leakage: A Comparative Study of Bulk and SOI Technologies," Proceedings of the *Design and Test in Europe (DATE)*, Mar. 2006, pp: 1-6.

C21. Arijit Raychowdhury, Ali Keshavarzi, Juanita Kurtin, Vivek De, and Kaushik Roy, "Optimal Spacing of Carbon Nanotubes in a CNFET Array for Highest Circuit Performance", Proceedings of the *Device Research Conference (DRC)*, Jun. 2006.

C22. Arijit Raychowdhury, and Kaushik Roy, "Using Super Cut-off Carbon Nanotube Sleep Transistors in Silicon Based Low Power Digital Circuits", Proceedings of the *IEEE Nano Conference*, Cincinnati, Jun. 2006.

C23. Mark Budnik, Arijit Raychowdhury, Kaushik Roy, "Power Delivery for Nanoscale Processors with Single Wall Carbon Nanotube Interconnects", Proceedings of the *IEEE Nano Conference*, Cincinnati, Jun. 2006.

C24. S. Ghosh, S. Bhunia, A. Raychowdhury, K. Roy, "Delay fault localization in test-per-scan BIST using built-in delay sensor," Proceedings of the *International On-Line Testing Symposium (IOLTS)*, Jul. 2006.

C25. Mark Budnik, Arijit Raychowdhury, Aditya Bansal and Kaushik Roy, "CNCAP: Design of a high density Carbon Nanotube Capacitor Structure", Proceedings of the *Design Automation Conference (DAC)*, Jul. 2006.

C26. A. Raychowdhury, Jeong Il Kim, D. Peroulis, and K. Roy, "Integrated MEMS Switches for Leakage Control of Battery Operated Systems", Proceedings of the *Custom Integrated Circuit Conference (CICC)*, Sep. 2006.

C27. Arijit Raychowdhury, Xunyao Fong, Qikai Chen, and Kaushik Roy, "Analysis of Super Cut-off Transistors for Ultralow Power Digital Logic Circuits", Proceedings of the *International Symposium of Low Power Electronic Design (ISLPED)*, Oct. 2006, pp: 1-6 (**Best paper award**).

C28. Arijit Raychowdhury, Ali Keshavarzi, Juanita Kurtin, Kaushik Roy, Vivek De "Scalability of Carbon Nanotube FET Circuits", in the Proceedings of the *Asian Solid State Circuits Conference (ASSCC)*, Nov. 2006, pp: 2-7.

C29. M-E. Hwang, Arijit Raychowdhury, Keejong Kim, and Kaushik Roy, "An 85mV 40nW Process-Tolerant Subthreshold 8X8 FIR Filter," Proceedings of the VLSI Circuits Symposium, Jun. 2007, pp: 154-155.

C30. Arijit Raychowdhury, Ali Keshavarzi, Vivek De, Shekhar Borkar, and Kaushik Roy, "The Theory of Multi-channel Carbon Nanotube Transistors for Variation Tolerant Digital Circuits," Proceedings of the *Device Research Conference (DRC)*, Mar. 2008.

C31. Arijit Raychowdhury, Charles Augustine, Yunfei Gao, Mark Lundstrom, and Kaushik Roy, "PETE: Purdue Emerging Technology Evaluator for estimating Power-Performance Trade-offs in Nanoscaled Circuits," *SRC TECHCON*, Nov. 2008.

C32. Y. William Li, Hasnain Lakdawala, Arijit Raychowdhury, Greg Taylor, K. Soumyanath, "A 1.05V 1.6mW, 0.45oC 3 Resolution based Temperature Sensor with Parasitic Resistance Compensation in 32nm Digital CMOS Process," Proceedings of the *International Solid State Circuit Conference (ISSCC)*, Feb. 2009.

C33. Charles Augustine, Arijit Raychowdhury, Yunfei Gao, Mark Lundstrom, Kaushik Roy, "PETE: A Device/Circuit Analysis Framework for Evaluation and Comparison Of Charge Based Emerging Devices," Proceedings of the *International Symposium on Quality Electron Design (ISQED)*, Mar. 2009 (**Nominated for best paper award**).

C34. Arijit Raychowdhury, Dinesh Somasekhar, Tanay Karnik, Vivek De, "Design Space and Scalability Exploration of 1T-1STT MTJ Memory Arrays in the Presence of Variability and Disturbances," Digest of *International Electron Device Meeting (IEDM)*, Dec. 2009.

C35. James Tschanz, Keith Bowman, Shih-Lien Lu, Paolo Aseron, Muhammad Khellah, Arijit Raychowdhury, Bibiche Geuskens, Carlos Tokunaga, Chris Wilkerson, Tanay Karnik, Vivek De, "A 45nm Resilient and Adaptive Microprocessor Core for Dynamic Variation Tolerance," Proceedings of the *International Solid State Circuit Conference (ISSCC)*, Feb. 2010.

C36. Arijit Raychowdhury, Bibiche Geuskens, Jaydeep Kulkarni, Jim Tschanz, Keith Bowman, Tanay Karnik, Shih-Lien Lu, Vivek De, Muhammad Khellah, "PVT & Aging Adaptive Word-Line Boosting for 8T SRAM Power reduction," Proceedings of the *International Solid State Circuit Conference (ISSCC)*, Feb. 2010.

C37. James Tschanz, Keith Bowman, Muhammad Khellah, Chris Wilkerson, Bibiche Geuskens, Dinesh Somasekhar, Arijit Raychowdhury, Jaydeep Kulkarni, Carlos Tokunaga, Shih-Lien Lu, Tanay Karnik, Vivek De, "Resilient Design in Scaled CMOS for Energy Efficiency", Proceedings of the *Asian & South Pacific Design Automation Conference (ASP-DAC)*, Feb. 2010.

C38. Jim Tschanz, Keith Bowman, Shih-Lien Lu, Paolo Aseron, Muhammad Khellah, Arijit Raychowdhury, Bibiche Geuskens, Carlos Tokunaga, Chris Wilkerson, Tanay Karnik, Vivek De, "On-Line Detection and Correction of Errors Due to Fast, Dynamic Voltage Droop Events," Digest of the *IEEE Workshop on Silicon Errors in Logic - System Effects*, Stanford University, Mar. 2010.

C39. Arijit Raychowdhury, Dinesh Somasekhar, Tanay Karnik, Vivek De, "Modeling and Analysis of Read (RD) Disturb in 1T-1STT MTJ Memory Bits", Proceedings of the *Device Research Conference (DRC)*, Mar. 2010.

C40. Arijit Raychowdhury, Bibiche Geuskens, Keith Bowman, James Tschanz, Shih-Lien Lu, Tanay Karnik, Muhammad Khellah, Vivek De, "Tunable Replica Bits for Dynamic Variation Tolerance in 8T SRAM," Proceedings of the *VLSI Circuit Symposium (VLSIC)*, Jun. 2010.

C41. Arijit Raychowdhury, "Model study of 1T-1STT MTJ Memory Arrays for Embedded Applications," Midwest Symposium on Circuits and Systems (MWCAS), Aug. 2010.

C42. Keith Bowman, James Tschanz, Shih-Lien Lu, Paolo Aseron, Muhammad Khellah, Arijit Raychowdhury, Bibiche Geuskens, Carlos Tokunaga, Chris Wilkerson, Tanay Karnik, Vivek De, "Resilient Microprocessor Design for High Performance and Energy Efficiency," Proceedings of the *International Symposium on Low Power Electronics & Design (ISLPED)*, Oct. 2010, pp: 355-355.

C43. M. Cho, N. Sathe, A. Raychowdhury, S. Mukhopadhyay, "Optimization of Burn-in Test for Many-core Processors through Adaptive Spatiotemporal Power Migration," Proceedings of the *International Test Conference (ITC)*, Nov. 2010.

C44. C. Augustine, A. Raychowdhury, D. Somasekhar, J. Tschanz, K. Roy, Vivek K. De, "Numerical Analysis of Typical STT-MTJ Stacks for 1T-1R Memory Arrays," Proceedings of the *International Electron Devices Meeting (IEDM)*, Dec. 2010.

C45. A. Raychowdhury, C. Augustine, D. Somasekhar, J. Tschanz, K. Roy, V. De, "Numerical analysis of a novel MTJ stack for high readability and writability," Proceedings of the *Solid-State Device Research Conference (ESSDERC)*, Jun. 2011.

C46. C. Augustine, A. Raychowdhury, B. Behin-Aein, S. Srinivasan, J. Tschanz, V. De, K. Roy, "Numerical analysis of domain wall propagation for dense memory arrays," Proceedings of the *IEEE International Electron Devices Meeting (IEDM)*, Dec. 2011.

C47. Michael Nicolaidis, Lorena Anghel, Yervant Zorian, Tanay Karnik, Keith Bowman, James Tschanz, Shih-Lien Lu, Carlos Tokunaga, Arijit Raychowdhury, Muhammad Khellah, Jaydeep Kulkarni, Vivek De, Dimiter Avresky, "Design for test and reliability in ultimate CMOS," Proceedings of *Design, Automation & Test in Europe (DATE)*, March 2012.

C48. Arijit Raychowdhury, Carlos Tokunaga, Willem Beltman, Michael Deisher, James Tschanz, Vivek De, "A 2.3nJ/Frame Voice Activity Detector for Context-Aware Systems in 32nm CMOS," Proceedings of the *Custom Integrated Circuit Conference (CICC)*, Jun. 2012.

C49. Arijit Raychowdhury, D. Somasekhar, J. Tschanz, V. De, "A fully-digital phase-locked low dropout regulator in 32nm CMOS," Proceedings of the *VLSI Circuit Symposium (VLSIC)*, Jun. 2012.

C50. Rangharajan Venkatesan, Vivek Kozhikkottu, Charles Augustine, Arijit Raychowdhury, Kaushik Roy and Anand Raghunathan, "TapeCache: A High Density, Energy Efficient Cache Based on Domain Wall Memory," Proceedings of the *International Symposium on Low Power Electronic Design (ISLPED)*, Jul. 2012 (**Best paper award**).

C51. A. Raychowdhury, "Pulsed READ in spin transfer torque (STT) memory bitcell for lower READ disturb," Proceedings of the *International Symposium on Nanoscale Architectures (NANOARCH)*, Jul. 2013.

C52. A. Raychowdhury, "Beyond charge based computation: Design space exploration of spin transfer torque based MRAMs for embedded applications," Proceedings of the *IEEE International Symposium on Low Power Electronics and Design (ISLPED)*, Oct. 2013.

C53. A. Raychowdhury, "Spin torque devices in embedded memory: model studies and design space exploration," Proceedings of the *International Conference on Computer-Aided Design (ICCAD)*, 572-575, Nov. 2013.

C54. C. Tokunaga, J. F. Ryan, C. Augustine, J. P. Kulkarni, Y-C. Shih, S. T. Kim, R. Jain, K. Bowman, A. Raychowdhury, M. M. Khellah, J. W. Tschanz, V. De, "A Graphics Execution Core in 22nm CMOS Featuring Adaptive Clocking, Selective Boosting and State-Retentive Sleep," Proceedings of the *International Solid State Circuits Conference (ISSCC)*, San Francisco, USA, Feb. 2014.

C55. **Samantak Gangopadhyay**, **YoungTak Lee**, **Saad B. Nasir**, Arijit Raychowdhury, "Modeling and Analysis of Digital Linear Dropout Regulators with Adaptive Control for High Efficiency under Wide Dynamic Range Digital Loads," Proceedings of the *Design, Automation & Test in Europe (DATE)*, Dresden Germany, March 2014.

C56. **Saad B. Nasir**, **YoungTak Lee**, Arijit Raychowdhury, "Modeling and Analysis of System Stability in a Distributed Power Delivery Network with Embedded Digital Linear Regulators," Proceedings of the *International Symposium on Quality Electronic Design (ISQED)*, San Jose, USA, March 2014.

C57. Suman Datta, Nikhil Shukla, Matthew Cotter, **Abhinav Parihar**, and Arijit Raychowdhury. "Neuro inspired computing with coupled relaxation oscillators," Proceedings of the *Annual Design Automation Conference*, pages 16, 2014.

C58. **Saad B. Nasir**, **Samantak Gangopadhyay** and Arijit Raychowdhury, "Adaptive Designs in Computation and Power Management," Proceedings of the *International Conference on Computer Aided Design (ICCAD)*, San Jose, Nov. 2014.

C59. N. Shukla, **Abhinav Parihar**, M. Cotter, M. Barth, X. Li, N. Chandrammorthy, D. G. Schlom, V. Narayanan, A. Raychowdhury, and S. Datta, "Pairwise Coupled Hybrid Vanadium Dioxide-MOSFET (HVFET) Oscillators for Non-boolean Associative Computing," Proceedings of the *IEEE International Electron Device Meeting (IEDM)*, December 2014.

C60. **Saad B. Nasir**, **Samantak Gangopadhyay** and A. Raychowdhury, "A 130nm fully digital linear dropout regulator with adaptive control and reduced dynamic stability for wide dynamic range of operation," Proceedings of the *International Solid State Circuits Conference (ISSCC)*, Feb 2015.

C61. **Saad B. Nasir** and A. Raychowdhury, "On limit cycle oscillations of discrete time digital linear regulators," Proceedings of the *IEEE Applied Power Electronics Conference (APEC)*, March 2015.

C62. **Samantak Gangopadhyay**, **Saad B. Nasir** and A. Raychowdhury, "Integrated Power Management in IoT Devices under Wide Dynamic Ranges of Operation," Proceedings of the *Design Automation Conference (DAC)*, June, 2015.

C63. **Anvesha Amravati**, **Manan Chung** and A. Raychowdhury, "A Time Interleaved DAC Sharing SAR Pipeline ADC for Ultra-Low Power Camera Front Ends," Proceedings of the *IEEE International Conference on Very Large Scale Integration (VLSI-SoC)*, October, 2015 (**Best Paper in Analog and Mixed-Signal Track**).

C64. **Saad Bin Nasir** and A. Raychowdhury, "Ensuring stability in a multi-LDO power grid for digital circuits through design and online tuning," Proceedings of the *Test and Validation of High Speed Analog Circuits (TVHSAC)*, October, 2015.

C65. **Ashwin Chintaluri**, **Abhinav Parihar**, Helia Naeimi, S. Natarajan and A. Raychowdhury, "A Model Study of Defects and Faults in Embedded Spin Transfer Torque (STT) MRAM Arrays," Proceedings of the *Asian Test Symposium (ATS)*, November, 2015.

C66. **Saad Bin Nasir** and A. Raychowdhury, "All-Digital Linear Regulators with Proactive and Reactive Gain-Boosting for Supply Droop Mitigation in Digital Load Circuits," Proceedings of the *International Symposium on Circuits and Systems (ISCAS)*, May, 2016.

C67. **Abhinav Parihar**, Nikhil Shukla, S. Datta and A. Raychowdhury, "Computing with Dynamical systems in the Post-CMOS Era," Proceedings of the *IEEE Summer Topicals Meeting*, July, 2016.

C68. Matthew Jerry, Wei-yu Tsai, Baihua Xie, Xueqing Li, Vijay Narayanan, Arijit Raychowdhury, and Suman Datta, "Phase Transition Oxide Neuron for Spiking Neural Networks," Proceedings of the *Device Research Conference*, June, 2016.

C69. **Anvesha Amravati**, Shaojie Xu. **Ningyuan Cao**, Justin Romberg and A. Raychowdhury, "A light-powered, "always on", smart camera with compressed domain gesture detection," Proceedings of the *International Symposium on Low Power Electronics and Design (ISLPED)*, Aug., 2016.

C70. **Saad B. Nasir** and Arijit Raychowdhury, "Hybrid Linear Regulator featuring Switched Model Control with 6ns/8.6mA Response Time and 98.64% Current Efficiency," *SRC TECHCON*, Sept., 2016.

C71. **Samantak Gangopadhyay** and Arijit Raychowdhury, "Unified Voltage and Frequency Regulator for Energy-Efficient Digital Circuits," *SRC TECHCON*, Sept., 2016.

C72. **Saad B. Nasir**, Shreyas Sen and Arijit Raychowdhury, "A 130nm Hybrid Low Dropout Regulator Based on Switched Mode Control for Digital Load Circuits," Proceedings of the *European Solid State Circuits Conference (ESSCIRC)*, Sept., 2016.

C73. **Samantak Gangopadhyay, Saad B. Nasir, A. Subramaniam**, V. Sathe and Arijit Raychowdhury, "UVFR: A Unified Voltage and Frequency Regulator with 500MHz/0.84V to 100KHz/0.27V Operating Range, 99.4%Current Efficiency and 27% Supply Guardband Reduction," Proceedings of the *European Solid State Circuits Conference (ESSCIRC)*, Sept., 2016.

C74. **Insik Yoon, Ashwin Chintaluri**, and Arijit Raychowdhury, "EMACS: Efficient MBIST Architecture for Test and Characterization of STT-MRAM Arrays" Proceedings of the *International Test Conference (ITC)*, Sept., 2016.

C75. **Saad Bin Nasir**, and Arijit Raychowdhury, "Embedded Hybrid LDO Topologies for Digital Load Circuits" Proceedings of the *Asia Pacific Conference on Circuits and Systems (APCCAS)*, Oct., 2016.

### B.3. Other Refereed Material

No data

### B.4. Submitted Journal Articles

No data

### B.5. Submitted Conference Articles (Refereed)

No data

## C. Other Publications and Creative Products

### C.1. Software

S1. "PETE: Purdue Emerging Technology Evaluator," http://nanohub.org/tools/pete/

*Short Description:* PETE was designed to evaluate any novel three terminal transistor for circuit level metrics. It used techniques for faster convergence and can also use incomplete, discontinuous and non-differential data points, which are often obtained experimentally. By providing a simple graphical interface and allowing researchers to provide tabulated I-V values for their experimental devices, this tool is useful for device scientists, material scientists and circuit designers. Due to its ease of use and

success in correctly predicting circuit level performance of several key transistor technologies, this tool was used as the benchmarking tool in the SRC and Federal Govt. sponsored, multi-university program, namely the Nanoelectronics Research Initiative (NRI) Program. All researchers in the NRI community used this tool to evaluate their respective devices against other technologies. Currently, this tool has 510+ users, and has logged more than 21.5K simulation runs.

### C.2. Patents

P1. Arijit Raychowdhury, Ali Keshavarzi, J. Kurtin, Vivek De, "Methods of forming carbon nanotube transistors for high speed circuit operation and structures formed thereby," US 11/648,209, 2006.

P2. Sandeep Oswal, Arijit Raychowdhury, Prakash E., Fernando Mujica, "DSL modem and method for reducing transmit echo therein," European Patent EP1333591, 2006.

P3. Sandeep Oswal, Arijit Raychowdhury, Prakash E., Fernando Mujica, "Adaptive Cancellation Network System And Method For Digital Subscriber Line", US Patent no. 7298838, 2007.

P4. S. Bhunia, H. Mahmoodi, A. Raychowdhury, S. Mukhopadhyay, K. Roy, "Low Power Scan Design and Delay Fault Testing Using First Level Supply Gating," US Patent no. 317319343, 2008.

P5. H. Lakhdawala, William Li, Gregory Taylor, Krishnamurthy Soumyanath, Arijit Raychowdhury, "Thermal Sensor Device," 8,096,707, 2008.

P6. Dia Khalil, Arijit Raychowdhury, Muhammad Khellah, Ali Keshavarzi, "Leakage Compoensation Circuit for Dynamic Random Access Memory Cells," US 7,961,498, 2008.

P7. Muhammad Khellah, B. Gueskens, Arijit Raychowdhury, "Method and System to Lower the Minimum Operating Voltage of a Memory Array," US 8,094,505, 2009.

P8. Mark Budnik, Arijit Raychowdhury, Aditya Bansal and Kaushik Roy, "High Density Capacitors for Integrated Circuit Technologies", US Patent no. 20070171594, 2009.

P9. Jaydeep Kulkarni, M. Khellah, B. Gueskens, Arijit Raychowdhury, T. Karnik, V. De, "Memory Write Operation Methods and Circuits," US 12/823,642, 2010.

P10. Arijit Raychowdhury, J. Kulkarni, James Tschanz, "Multi-Supply Sequential Logic Unit," US 101143110, 2010.

P11. Brian Doyle, Arijit Raychowdhury, Yong Ju, Charles Kuo, Oguz Kaan, David Kencke, R. Chau, R. Golizadeh, "Memory with Elements Having Two Stacked Magentic Tunneling Junctions Devices," PCT/ US2011/ 066979, 2011.

P12. Arijit Raychowdhury, J. Kulkarni, James Tschanz, "Multi-Supply Sequential Logic Unit," PCT/ US2011/ 064848, 2011.

P13. Charles Kuo, B. Doyle, Arijit Raychowdhury, R. Golizadeh, Oguz Kaan, "Balancing Energy Barrier Between States in Perpendicular Magnetic Tunnel Junctions," PCT/ US2011/ 068158, 2011.

P14. Marco Beltman, Matias Zanartu, Arijit Raychowdhury, Anand Rangarajan, Michael Deisher, "Speech Audio Processing," US 10-2012-7031843, 2011.

P15. Marco Beltman, Matias Zanartu, Arijit Raychowdhury, Anand Rangarajan, Michael Deisher, "Speech Audio Processing," PCT/US2011/042515, 2011.

P16. Jaydeep Kulkarni, M. Khellah, B. Gueskens, Arijit Raychowdhury, T. Karnik, V. De, "Memory Write Operation Methods and Circuits," PCT/US2011/040458, 2011.

P17. Arijit Raychowdhury, Marco Beltman, James Tschanz, Carlos Tokunaga, Mike Deisher, Tomas Walsh, "Low Power Voice Detection," PCT/US2011/063622, 2011.

P18. Arijit Raychowdhury, Charles Augustine, James Tschanz, Vivek De, "A Digital Clamp for State Retention in Embedded Sequentials," Filed with the USPTO, 2012.

P19. Arijit Raychowdhury, James Tschanz, Vivek De, "Spin Transfer Torque Based Memory Elements for Programmable Device Arrays," PCT/US2012/031371, 2012.

P20. Arijit Raychowdhury, Dinesh Somasekhar, James Tschanz, Vivek De, "Digitally Phase Locked Low Drop-out Regulator," PCT/US2012/057066, 2012.

P21. Arijit Raychowdhury, B. Doyle, David Kencke, Charles Kuo, James Tschanz, Fatih Hamazaoglu, Eric Wang, R. Golizadeh, "Methods and Systems to Read a Magnetic Tunnel Junction Based Memory Cell Based on a Pulsed Read Current," PCT/US2012/030490, 2012.

## D. Presentations

### D.1 Technical Panel Participation and Presentation

1. "Analog IP: Is there any scope in the fragmented and commoditized market?" Workshop on Test and Verification of High Speed Analog Circuits, Los Angeles, Oct. 2015.

### D.2 Invited Seminar Presentations

1. "Designing with Subthreshold logic: From Devices to Systems," University of Florida, Gainesville Florida, Mar. 2007.
2. "Subthreshold Design: Prospects and Challenges," University of Waterloo, Waterloo Canada, Apr. 2007.
3. "Carbon Nanotube Electronics: Modeling, Circuit Implications, and Challenges," University of Michigan, Ann Arbor, May 2007.
4. "Designing Adaptive and Resilient Digital Systems," Invited Speaker Series, University of Washington, Washington, USA, Oct. 2010.
5. "High-Efficiency On-Die Digital Linear Voltage Regulators with On-Line Adaptation for Loads with Wide Dynamic Range of Operation," Qualcomm Inc., Raleigh, USA, Oct. 2013.
6. "Linear Regulation: The Role of Adaptive Control", Intel Corporation, Hillsboro, OR, Nov. 2013.
7. "Voltage Regulators for Wide Dynamic Range", IBM T. J. Watson Research Lab, NY, Oct. 2014.
8. "Control Strategies for Linear Regulators in On-die Voltage Regulation of Digital Load Circuits", Qualcomm Research lab, Raleigh, NC, Nov. 2015.
9. "Enabling Fine-grained Power Management through Distributed On-Die Voltage Regulators", Keysight Technologies Research Lab, San Jose, CA, Nov. 2015.
10. "On-die Regulators for Fine-grained Power Management: Digital and Hybrid Topologies with Advanced Control Techniques", Intel Labs, Hillsboro, OR, May 2016.
11. "Computing with Dynamical Systems", IEEE Summer Topicals Meeting, Newport Beach, CA, July 2016.

### D.3 Tutorial Presentations

1. "Model study of 1T-1STT MTJ Memory Arrays for Embedded Applications," Midwest Symposium on Circuits and Systems (MWCAS), Aug. 2010.
2. "Design Considerations for 1T-1STT MTJ Based Embedded Memory Arrays," CSIS International Symposium on Spintronics Based VLSI, Sendai, Japan, Feb. 2011.
3. 1T-1STT MTJ Memory Arrays for Embedded Applications," Non-volatile Memory Workshop, San Diego, USA, March 2011.
4. "1T-1STT MTJ Based Embedded Memory Arrays," Spintronics Workshop on LSI, Hawaii, USA, Jun. 2012.
5. "Spintronics for Embedded Non-volatile Electronics," International Electron Device Meeting (IEDM), San Francisco, USA, Dec. 2012.
6. "Adaptive SRAM Circuits," Design and Test in Europe (DATE), Grenoble, France, Mar. 2013.
7. "Spintronics for Embedded Memory: A Model Study," International Symposium on Low Power Electronic Design, Oct. 2013.
8. "Computing with Spin: Beyond Charge Based Electronics," International Conference on Computer Aided Design (ICCAD), Nov. 2013.
9. "Adaptive and Resilient Circuits for Improving Energy Efficiency in Wide Dynamic Range Digital Systems," IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S), Monterey Bay, USA, Oct. 2013.
10. "Adaptive Designs in Computation and Power Management," International Conference on Computer Aided Design (ICCAD), San Jose, Nov. 2014.
11. "On Die Digital Voltage Regulators with Continuous Time and Discrete Time Control for Loads with Wide Dynamic Range of Operation," IEEE International Conference on Integrated Circuit Design and Technology (ICICDT), Austin, May 2014.
12. "Integrated power management in IoT devices under wide dynamic ranges of operation," Design Automation Conference (DAC), June 2015
13. "Digitizing On-die Regulators: A Scaling Perspective," International Symposium on Quality Electronic Design (ISQED), March 2016.
14. "Always ON Sensors for the Internet of Smart Things," Design Automation Conference (DAC), June 2016

## E. Grants and Contracts

### E.1 As Principal Investigator

1. **Title: E2CDA: Extremely Energy Efficient Collective ELectronics (EXCEL)**
   Agency/Company: NSF: 60% and SRC: 40%
   Amount: *USD 4,419,225*
   Role: *GT-PI; Center Director: S. Datta (Univ of Notre Dame)*
   Collaborator(s): J. Romberg, S. Vempala, S. Datta, Z. Toroczai
   Period of Contract: *10/01/2017-09/30/2019*
   Candidate's Share: *11% (USD 480,000)*

2. **Title: Unification of Voltage Regulation and High Performance Clocking Circuits**
   Agency/Company: Qualcomm Inc.
   Amount: *USD 70,000*
   Role: *PI*
   Collaborator(s): None
   Period of Contract: *07/01/2016-06/31/2017*
   Candidate's Share: *100%*

3. **Title: Architecting STT-RAM to Address and Exploit Variability**
   Agency/Company: Samsung Semiconductor USA
   Amount: *USD 150,000*
   Role: *PI*
   Collaborator(s): Moinuddin Qureshi
   Period of Contract: *07/15/2016-07/14/2018*
   Candidate's Share: *50%*

4. **Title: Early Career Faculty Award**
   Agency/Company: Intel Corporation
   Amount: *USD 25,000*
   Role: *PI*
   Collaborator(s): None
   Period of Contract: *No limit*
   Candidate's Share: *100%*

5. **Title: Switched Mode Control and Load Balancing in Distributed Linear Regulators for Fine-Grained Spatiotemporal Power Management**
   Agency/Company: Keysight Technologies
   Amount: *USD 30,000*
   Role: *PI*
   Collaborator(s): None
   Period of Contract: *Jan. 2016 - Dec. 2016*
   Candidate's Share: *100%*

6. **Title: CRII: SHF: Real-time Approximate-Dynamic-Programming based Neuro-controllers for Dynamic Power Management in Power-Constrained Digital Systems**
   Agency/Company: National Science Foundation
   Amount: *USD 254,000 (includes GT cost share)*
   Role: *PI*
   Collaborator(s): None
   Period of Contract: *September 2015 - August 2017*
   Candidate's Share: *100%*

7. **Title: Models, Algorithms and BIST Hardware Development for Manufacturing & Characterization Tests of Spin-Transfer-Torque MRAM Arrays**
   Agency/Company: Semiconductor Research Corporation
   Amount: *USD 195,000*
   Role: *PI*
   Collaborator(s): None
   Period of Contract: *December 2013 - November 2016*
   Candidate's Share: *100%*

8. **Title: Embedded & Adaptive Voltage Regulators with Proactive Noise Reduction for Digital Loads under Wide Dynamic Range**
   Agency/Company: Semiconductor Research Corporation

Amount: *USD 255,000*
Role: *PI*
Collaborator(s): None
Period of Contract: *February 2014 - January 2017*
Candidate's Share: *100%*

9. **Title: Next Generation Power Management with Embedded All-Digital Voltage Regulators**
Agency/Company: Intel Corporation
Amount: *USD 360,000*
Role: *PI*
Collaborator(s): None
Period of Contract: *December 2014 - November 2017*
Candidate's Share: *100%*

10. **Title: Hybrid Analog and Digital LDO VR for Fast Transient Response and High Steady-State Current Efficiency Project**
Agency/Company: Qualcomm Inc.
Amount: *USD 70,000*
Role: *PI*
Collaborator(s): None
Period of Contract: *May 2015 - April 2016*
Candidate's Share: *100%*

11. **Title: On-Die Load-Adaptive Voltage Regulator (VR) for Energy-Efficient Processor Design**
Agency/Company: Qualcomm Inc.
Amount: *USD 60,000*
Role: *PI*
Collaborator(s): None
Period of Contract: *March 2014 - April 2015*
Candidate's Share: *100%*

12. **Title: Gesture Based Wakeup in an Always-On & Always-Connected Camera System using Algorithm-Hardware Co-Design in the Compressed Domain**
Agency/Company: Intel Corporation
Amount: *USD 240,000*
Role: *PI*
Collaborator(s): Justin Romberg
Period of Contract: *August 2014 - July 2017*
Candidate's Share: *50% (USD 120,000)*

13. **Title: Design and Analysis of Digital Low-Dropout Regulators for Fine-Grained and Embedded Power Management**
Agency/Company: Intel Corporation
Amount: *USD 70,000*
Role: *PI*
Collaborator(s): None
Period of Contract: *June 2013 - May 2014*
Candidate's Share: *100%*

14. **Title: Algorithms and Hardware for Matching and Recognition**
Agency/Company: Intel Corporation
Amount: *USD 75,000*
Role: *PI*
Collaborator(s): None

Period of Contract: *March 2013 - April 2014*
Candidate's Share: *100%*

15. **Title: Low-power FPGA Implementation of Boltzman Machines**
Agency/Company: Xilinx Corporation
Amount: *In Kind Gift priced at USD 4,500*
Role: *PI*
Collaborator(s): None
Period of Contract: *July 2013*
Candidate's Share: *100%*

### E.2 As Co-Principal Investigator

1. **Title: Integrated Voltage Regulators for On-die Power Management**
Agency/Company: Power Delivery in Electronic Systems (PDES) - an Industry Consortium
Amount: *USD 840,000*
Role: *co-PI*
PI(s): Madhavan Swaminathan
Other Collaborator(s): S. Mukhopadhyay, H. Wang, P. Kohl
Period of Contract: *Oct. 2015-Sept. 2017 (Phase-I)*
Candidate's Share: *14% (USD 120,000) including fabrication cost*

### E.3 As Senior Personnel or Contributor

No data

### E.4 Pending Proposals

No Data

## F. Other Scholarly and Creative Accomplishments

No data

## G. Societal and Policy Impacts

No data

## H. Other Professional Activities

No data

# V. Teaching

## A. Courses Taught

| Semester/Year | Course Number | Course Title | Enrollment |
|---|---|---|---|
| Spring 2013 | ECE4130A | Advanced VLSI Systems | 11 |
| Spring 2013 | ECE6130A | Advanced VLSI Systems | 52 |
| Summer 2013 | ECE 2020A | Fundamentals of Digital System Design | 35 |

| Semester/Year | Course Number | Course Title | Enrollment |
|---|---|---|---|
| Fall 2013 | ECE 2020A | Fundamentals of Digital System Design | 48 |
| Spring 2014 | ECE8893 | Digital Design using Modern VLSI Devices | 34 |
| Summer 2014 | ECE 2020A | Fundamentals of Digital System Design | 36 |
| Fall 2014 | ECE4130A | Advanced VLSI Systems | 17 |
| Fall 2014 | ECE6130A | Advanced VLSI Systems | 92 |
| Spring 2015 | ECE4130A | Advanced VLSI Systems | 5 |
| Spring 2015 | ECE6130A | Advanced VLSI Systems | 51 |
| Summer 2015 | ECE 2020A | Fundamentals of Digital System Design | 36 |
| Fall 2015 | ECE8893 | Digital Design using Modern VLSI Devices | 5 |
| Fall 2015 | ECE 2020A | Fundamentals of Digital System Design | 52 |
| Spring 2016 | ECE4130A | Advanced VLSI Systems | 5 |
| Spring 2016 | ECE6130A | Advanced VLSI Systems | 11 |
| Summer 2016 | ECE3030 | Physical Foundations of Computing | 25 |
| Fall 2016 | ECE2020A | Fundamentals of Digital System Design | 25 |
| Fall 2016 | ECE2020B | Fundamentals of Digital System Design | 25 |

## B. Individual Student Guidance

### B.1a Ph.D. Students (In Process)

1. Samantak Gangopadhyay, PhD Student, ECE
   Fall 2013 to present
   Current Status: Passed Preliminary Exam in Fall 2013
   Topic: A Flexible On-die Power Delivery Fabric for Low-Power Multi-core Systems
   Key Publications : DATE'14, JSSC'14, ISSCC'15, DAC'15, ESSCIRC'16
   Other remarks: Finalist for Qualcomm Innovation Fellowship 2015

2. Saad Bin Nasir, PhD Student, ECE
   Fall 2013 to present
   Current Status: Passed Preliminary Exam in Fall 2013
   Topic: Adaptive and Switched Mode Control in Linear Regulators for Digital Load Circuits
   Key Publications : TPE'16, ISSCC'15, APEC'15, DATE'14, DAC'15, ESSCIRC'16
   Other remarks: Finalist for Qualcomm Innovation Fellowship 2015

3. Abhinav Parihar, PhD Student, ECE
   Fall 2013 to present
   Current Status: Passed Preliminary Exam in Fall 2013
   Topic: Computation with Coupled Dynamical Systems
   Key Publications : NATURE SR'14, IEDM'14, JAP'15, JETCAS'14

4. Anvesha Amravati, PhD Student, ECE
   Fall 2014 to present
   Current Status: Passed Preliminary Exam in Fall 2014
   Topic: Always-On Sensor Nodes with Compressive Domain Data Acquisition

Key Publications : ISLPED'16, VLSI SOC'15
Other remarks: Best Paper in Analog/Mixed-Signal Track (VLSI-SOC Conference)

5. Insik Yoon, PhD Student, ECE
   Fall 2015 to present
   Current Status: Passed Preliminary Exam in Spring 2016
   Topic: Spin Transfer Torque Based Memory Systems

6. Ningyuan Cao, PhD Student, ECE
   Fall 2015 to present
   Current Status: Passed Preliminary Exam in Fall 2015
   Topic: Power Management in IoT Devices
   Key Publications : ISLPED'16

**B.2a M.S. Students (In Process)**

1. Anirudha Kurkhade, M.S. Student with Thesis, ECE
   Spring 2015 to present (Expected Graduation in Spring 2016)
   Topic: Phase Transition Materials in Spiking Neural Circuits

**B.2b M.S. Students (Graduated with Thesis)**

1. Ashwin Chintaluri, M.S. Student with Thesis, ECE
   Fall 2014 to Spring 2016
   Topic: Analysis of Defects and Fault Models in Embedded STT-MRAM Arrays
   First Employment: Microsoft Corporation, WA

2. Ashwin Subramanium, M.S. Student with Thesis, ECE
   Fall 2014 to Fall 2015
   Topic: Resilient Digital Circuits with Efficient Clock-Data Compensation
   First Employment: Apple Corporation, CA

3. Soham Desai, M.S. Student with Thesis, ECE
   Fall 2013 to Spring 2015 (Graduation)
   Topic: Hardware Implementation of Reconfigurable Restricted Boltzmann Machines for Image Recognition
   First Employment: Intel Labs, OR

**B.2c M.S. Students (Graduated non-Thesis)**

1. Zhilun Li, M.S. Student, ECE
   Spring 2013 to Spring 2014 (Graduation)
   Topic: Energy-Accuracy Trade-offs in Compressive Sensing Cameras
   First Employment: Oracle, CA

2. Youngtak Lee, M.S. Student, ECE
   Spring 2013 to Fall 2014 (Graduation)
   Topic: Low Drop-out Digital Regulators
   First Employment: PreScouter Inc., GA
   Publications: ISQED'14, DATE'14

### B.3 Undergraduate Students (In Process)

1. Sitong Wu, B.S. Student, ECE
   Summer, Fall 2016
   Topic: ASIC support for deep learning

2. Chirag Medpara, B.S. Student, ECE
   Spring 2016
   Topic: ASIC support for deep learning

3. Soham Roy, B.Tech. Student, EE, Indian Institute of Tech, Delhi
   Summer 2016
   Topic: Switched Mode Fast Locking Phase Locked Loops

### B.4 Service on Thesis or Dissertation Committees

#### B.4a Internal (Georgia Tech)

| Student | Advisor | School | Date of Graduation |
|---|---|---|---|
| Khondker Zakir Ahmed | Prof. Saibal Mukhopadhyay | School of ECE | July 2016 |
| Jayaram Natarjan | Prof. Abhijit Chatterjee | School of ECE | May 2016 |
| Taigon Song | Prof. Sung Kyu Lim | School of ECE | Oct. 2015 |
| Sergio Carlos | Prof. Saibal Mukhopadhyay | School of ECE | Oct. 2015 |
| Amit Trivedi | Prof. Saibal Mukhopadhyay | School of ECE | Sep. 2015 |
| Boris Alexandrov | Prof. Saibal Mukhopadhyay | School of ECE | Aug. 2015 |
| Wen Yuen | Prof. Saibal Mukhopadhyay | School of ECE | Aug. 2015 |
| Shreepad Pant | Prof. Sung Kyu Lim | School of ECE | Apr. 2015 |
| Satyan Telikepalli | Prof. Swaminathan Madhavan | School of ECE | May 2015 |
| Xian Wang | Prof. Abhijit Chatterjee | School of ECE | Dec. 2014 |
| Kwanyeob Chae | Prof. Saibal Mukhopadhyay | School of ECE | Aug. 2013 |

#### B.4b External

| Student | University | Advisor | Date of Graduation |
|---|---|---|---|
| Rangharajan Venkatesan | Purdue University | Prof. A. Raghunathan | Summer 2014 |
| Sumeet K. Gupta | Purdue University | Prof. K. Roy | Summer 2012 |
| Charles Augustine | Purdue University | Prof. K. Roy | Summer 2011 |

## C. Other Teaching Activities

### C.1 Course Development

**ECE8893 Digital Design using Modern VLSI Devices:** This is a graduate-level course on the fundamentals of nano-scaled electron devices and their role in digital VLSI design. Dr. Raychowdhury developed this course to

provide an overview of both the fundamentals of digital VLSI devices in terms of their electrostatic and transport properties, as well as to cover the state of the art design techniques that address some of the device level challenges. The course has assignments and a project. Students are taught how to think of MOSFETs intuitively and what the major device breakthroughs in the last ten technology nodes have been. In the second half of the course, the students are exposed to advanced VLSI design techniques that address critical challenges like increased transistor leakage, excessive device parameter variation as well as design topologies that are resilient to variation and noise.

### C.2 Course Improvement

1. Worked with Prof. Sudhakar Yalamanchili to introduce the concepts of delay and energy dissipation in ECE 2020. This provides the students with foundational understanding of the different trade-offs in digital systems and what the growing challenges in digital design are.
2. Introduced the notion of energy efficient design in ECE6130/4130 through a revamped project assignment. Super-threshold, near-threshold and sub-threshold designs are now explored in details to meet the current demand of the industry.

### C.3 Professional Development/Continuing Education

No data

### C.4 Other Teaching Activities

No data

# VI. Service

## A. Professional Contributions

### A.1 Editorial

**Associate Editor** *IEEE Transactions on Computer Aided Design*, 2015 - present

**Editor** *Microelectronics Journal*, 2014 - present

**Guest Editor** *ACM Journal on Emerging Technologies in Computing Systems: Special Issue on Emerging Memory Technologies*, May 2013

### A.2 Memberships and Activities in Professional Societies

1. Panel Member and Member of Selection Committee for Senior Members, The Institute of Electrical and Electronics Engineers (IEEE) South-East Region
2. Senior Member, The Institute of Electrical and Electronics Engineers (IEEE)
3. Member, The Association for Computing Machinery (ACM)

### A.3 Organization and Chairmanship of Technical Sessions, Workshops, and Conferences

1. **Tutorial Chair**, International Symposium on Quality Electronic Design (ISQED) 2014, 2015
2. **Track Chair**, VLSI Conference 2014, 2015;
3. **Track Chair**, International Conference on Computer Aided Design (ICCAD) 2010, 2011

**Membership in Conference Technical Committee**

1. Design Automation and Test in Europe (DATE) 2017
2. Custom Integrated Circuits Conference (CICC) 2015
3. Workshop on Test & Verification of High Speed Analog Circuits (TVHSAC) 2015
4. Design Automation Conference (DAC) 2014, 2013, 2012
5. International Symposium on Low Power Electronic Design (ISLPED) 2016, 2015, 2014, 2013
6. International Conference on Computer Aided Design (ICCAD) 2012, 2011, 2010, 2009, 2008
7. International Symposium on Quality Electronic Design (ISQED) 2016, 2015, 2014, 2013, 2012, 2011, 2010, 2009, 2008
8. VLSI Conference 2014, 2011, 2010

### A.4 Technical Journal and Conference Referee

1. *IEEE Journal of Solid State Circuits (JSSC)*
2. *IEEE Transactions on VLSI Systems (TVLSI)*
3. *IEEE Transactions on Electron Devices(TED)*
4. *IEEE Transactions on Circuits and Systems (TCAS) I & II*
5. *IEEE Transactions on Computer Aided Design (TCAD)*
6. *IEEE Transactions on Nanotechnology (TNANO)*
7. *IEE Proceedings - Circuits, Devices and Systems*
8. *Microelectronics Journal*
9. International Symposium on Low Power Electronics and Design (ISLPED)
10. International Symposium on Quality Electronic Design (ISQED)
11. International Symposium on Circuits and Systems (ISCAS)
12. International SOC Design Conference (ISOCC)
13. Design Automation Conference (DAC)
14. Custom Integrated Circuits Conference (CICC)
15. International Conference on Computer Aided Design (ICCAD)

### A.5 Proposal Panel Reviews

1. Panelist, National Science Foundation, CISE Directorate, April 2016
2. Panelist, National Science Foundation, CISE Directorate, Dec 2015
3. Panelist, National Science Foundation, CISE Directorate, Jan 2010
4. Reviewer & Panelist, Semiconductor Research Corporation (Global Research Council), 2011

### A.6 Other Involvement

| | |
|---|---|
| Technical Contributor | International Technology Roadmap for Semiconductors, 2010-2012 Editions |
| Industry Liaison | Emerging Technologies Theme, C2S2 Center, FCRP, 2008-2012 |
| Industry Mentor | Several SRC Projects, Nano-electronics Research Initiative (NRI) |

## B. Public and Community Service

No data

## C. Institute Contributions

### C.1 Institute Committee Service

No Data

### C.2 College Committee Service

No data

### C.3 School Committee Service

1. Graduate Committee, 2014-2015
2. Graduate Committee, 2015-2016

### C.4 Program Development: Research

No data

### C.5 Program Development: Academic

No data

### C.6 Other Institute Service Contributions

No data