Tushar **Krishna**

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PHONE (+1) 206 601 6213 • **E-MAIL** tushar@ece.gatech.edu • **WEB** http://tusharkrishna.ece.gatech.edu

RESEARCH INTERESTS

Computer Architecture: multicore, parallel, heterogeneous, spatial, ML accelerators, FPGA
Interconnection Networks: Networks-on-Chip, HPC switches, data-centers, sensor networks

EDUCATION

Feb 2014 **Massachusetts Institute of Technology**
Ph.D. in Electrical Engineering and Computer Science
- *Advisor:* Li-Shiuan Peh
- *Committee:* Srinivas Devadas and Joel Emer
- *Thesis:* "Enabling Dedicated Single-Cycle Connections Over A Shared Network-on-Chip"

Sep 2009 **Princeton University**
M.S.E. in Electrical Engineering
- *Advisor:* Li-Shiuan Peh
- *Thesis:* "Networks-on-Chip with Hybrid Interconnects"

Aug 2007 **Indian Institute of Technology (IIT), Delhi**
B.Tech. (Honors) in Electrical Engineering

PROFESSIONAL EXPERIENCE

Aug '15 – present **Georgia Institute of Technology,** Atlanta, GA, USA
Assistant Professor
School of Electrical and Computer Engineering.
School of Computer Science (Adjunct).

Feb '15 – Jul '15 **Massachusetts Institute of Technology, SMART Center,** Cambridge, MA, USA
Post-doctoral Researcher.

Nov '13 – Jan '15 **Intel Corporation, VSSAD Group**, Hudson, MA
Research Engineer. Manager: Joel Emer

Jun'10 – Aug '10 **AMD (Advanced Micro Devices) Research**, Bellevue, WA, USA
Co-Op Engineer. Mentors: Bradford Beckmann and Steve Reinhardt

Jun'09 – Aug '09 **AMD Research**, Bellevue, WA, USA
Co-Op Engineer. Mentors: Bradford Beckmann and Steve Reinhardt

Jun'08 – Aug '08 **AMD,** North Bridge Architecture Group, Sunnyvale, CA, USA
Co-op Engineer. Mentor: Pat Conway

May'06 – Jul '06 **NVIDIA**, Digital Hardware Design Group, Bangalore, India
Summer Intern.

BOOKS

"On-Chip Networks", Second Edition
Natalie Enright Jerger, **Tushar Krishna**, and Li-Shiuan Peh.
Synthesis Lectures on Computer Architecture. Morgan & Claypool Publishers. June 2017

HONORS AND AWARDS

2018	**NSF CISE Research Initiation Initiative (CRII) Award**
2017	**Best Paper Award** (Design Methods & Tools) at Design Automation and Test in Europe (DATE)
2014	**Best Paper Award** at the 8th International Symposium on Networks-on-Chip (NOCS)
2014	**IEEE Micro Top Picks** from Computer Architecture Conferences
2009	**IEEE Micro Top Picks** from Hot Interconnects
2007-08	**Princeton Graduate Fellowship**
2007	ICIM Stay Ahead Award for the **Best Undergraduate Project in Computer Technology**, IIT Delhi
2004-2006	"National Initiative for Undergraduate Sciences" (NIUS) Fellowship, Homi Bhabha Centre for Science Education (HBCSE), India
2003, 2004	Merit prize for academic excellence, IIT Delhi
2003	**Gold Medal** at the Indian National Chemistry Olympiad – one of top 25 Indians

RESEARCH FUNDING

NSF: CRII (Jan'18 – Dec'19)	Enabling Neuroevolution in Hardware. **PI: Tushar Krishna**, $175,000
DARPA: CHIPS (Aug'17 - Aug'21)	A Vertically Integrated Flow for IP Reuse and Heterogeneous Integration PI: Sungkyu Lim, **Co-PIs: Tushar Krishna**, Saibal Mukhopadhyay, Madhavan Swaminathan $3.7M

PUBLICATIONS (REFEREED JOURNALS)

JSSC 2017 ***528 citations***	"Eyeriss: An Energy-Efficient Reconfigurable Accelerator for Deep Convolutional Neural Networks" Yu-Hsin Chen, **Tushar Krishna**, Joel Emer, and Vivienne Sze *IEEE Journal of Solid State Circuits Conference, ISSCC Special Issue, Jan 2017*
TOCS 2015	"Efficient Control and Communication Paradigms for Coarse-Grained Spatial Architectures" M. Pellauer, A. Parashar, M. Adler, B. Ahsan, R. Allmon, N. Crago, K. Fleming, M. Gambhir, A. Jaleel, **T. Krishna**, D. Lustig, S. Maresh, V. Pavlov, R. Rayess, A. Zhai, and J. Emer *ACM Transactions on Computer Systems, Sep 2015*
IEEE Micro Top Picks 2014	"SMART: Single-Cycle Multihop Traversals Over A Shared Network-on-Chip" **Tushar Krishna**, Chia-Hsin Owen Chen, Woo-Cheol Kwon, and Li-Shiuan Peh *IEEE Micro (**Special Issue: Top Picks from the Computer Architecture Conferences**), May/Jun 2014*
IEEE Computer 2013 ***Webex Chat with Guest Editor:*** youtu.be/k_I8yc_CjBU	"Single-Cycle Multihop Asynchronous Repeated Traversal: A SMART Future for Reconfigurable On-Chip Networks" **Tushar Krishna**, Chia-Hsin Owen Chen, Sunghyun Park, Woo-Cheol Kwon, Suvinay Subramanian, Anantha P. Chandrakasan, and Li-Shiuan Peh *IEEE Computer, 46(10): 48-55, Oct 2013*
TVLSI 2012	"SWIFT: A Low-Power Network-On-Chip Implementing the Token Flow Control Router Architecture With Swing-Reduced Interconnects" Jacob Postman, **Tushar Krishna**, Christopher Edmonds, Li-Shiuan Peh, and Patrick Chiang *IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 21(8): 1432-1446, Aug 2012*
CAN 2011 ***2737 citations***	"The gem5 simulator" N. Binkert, B. Beckmann, G. Black, S. K. Reinhardt, A. Saidi, A. Basu, J. Hestness, D. R. Hower, **T. Krishna**, S. Sardashti, R. Sen, K. Sewell, M. Shoaib, N. Vaish, M. D. Hill and D. A. Wood *SIGARCH Computer Architecture News, 39(2): 1-7, May 2011*

IEEE Micro Top Picks 2009 "Express Virtual Channels with Capacitively-Driven Global Links"
Tushar Krishna, Amit Kumar, Jacob Postman, Patrick Chiang, Mattan Erez, and Li-Shiuan Peh
*IEEE Micro (**Special Issue: Top Picks from Hot Interconnects 16**), 29 (4): 48-61, Jul/Aug 2009*

PUBLICATIONS (REFEREED CONFERENCES)

ICRC 2018 Merge Network for a Non-von Neumann Accumulate Accelerator in a 3D Chip
Anirudh Jain, Sriseshan Srikanth, Erik Debenedictis, and **Tushar Krishna**
In Proc of 3rd IEEE International Conference on Rebooting Computing, Nov 2018

MICRO 2018 GeneSys: Enabling Continuous Learning through Neural Network Evolution in Hardware
Ananda Samajdar, Parth Mannan, Kartikay Garg, and **Tushar Krishna**
In Proc of 51st Annual IEEE/ACM International Symposium on Microarchitecture, Oct 2018

MICRO 2018 Scalable Distributed Last-Level TLBs Using Low-Latency Interconnects
Srikant Bharadwaj, Guilherme Cox, **Tushar Krishna**, and Abhishek Bhattacharjee
In Proc of 51st Annual IEEE/ACM International Symposium on Microarchitecture, Oct 2018

NOCS 2018 Brownian Bubble Router: Enabling Deadlock Freedom via Guaranteed Forward Progress
Mayank Parasar, Ankit Sinha, and **Tushar Krishna**
In Proc of 11th International Symposium on Networks-on-Chip, Oct 2018

NOCS 2018 Architecting a Secure Wireless Network-on-Chip
Brian Lebiednik, Sergi Abadal, Hyouk Jun Kwon and **Tushar Krishna**
In Proc of 11th International Symposium on Networks-on-Chip, Oct 2018 (Special Session Paper)

ISCA 2018 Synchronized Progress in Interconnection Networks (SPIN) : A New Theory for Deadlock Freedom
Aniruddh Ramrakhyani, Paul Gratz, and **Tushar Krishna**
In Proc of 45th International Symposium on Computer Architecture, Jun 2018

ISCA 2018 "FastTrack: Leveraging Heterogeneous FPGA Wires to Design Low-cost High-performance Soft NoCs"
Nachiket Kapre and **Tushar Krishna**
In Proc of 45th International Symposium on Computer Architecture, Jun 2018

ISCA 2018 "SEESAW: Using Superpages to Improve VIPT Caches"
Mayank Parasar, Abhishek Bhattacharjee, and **Tushar Krishna**
In Proc of 45th International Symposium on Computer Architecture, Jun 2018

ISPASS 2018 "Performance Implications of NoCs on 3D-Stacked Memories: Insights from the Hybrid Memory Cube"
Ramyad Hadidi, Bahar Asgari, Jeffrey Young, Burhan Ahmad Mudassar, Kartikay Garg, **Tushar Krishna**, and Hyesoon Kim
In Proc of the IEEE Int. Symp on Performance Analysis of Systems and Software, Apr 2018

ASPLOS 2018 "MAERI: Enabling Flexible Dataflow Mapping over DNN Accelerators via Reconfigurable Interconnects"
Hyoukjun Kwon, Ananda Samajdar, and **Tushar Krishna**
In Proc of the 23rd ACM International Conference on Architectural Support for Programming Languages and Operating Systems, Mar 2018

ASPLOS 2018 "LATR: Lazy Translation Coherence"
Mohan Kumar, Steffen Maass, Sanidhya Kashyap, Jan Vesely, Zi Yan, Taesoo Kim, Abhishek Bhattacharjee, and **Tushar Krishna**
In Proc of the 23rd ACM International Conference on Architectural Support for Programming Languages and Operating Systems, Mar 2018

SysML 2018 "MAERI: Enabling Flexible Dataflow Mapping over DNN Accelerators via Programmable Interconnects"
Hyoukjun Kwon, Ananda Samajdar, and **Tushar Krishna**
In Inaugural SysML Conference, Feb 2018

AISTECS 2018 "Spoofing Prevention via RF Power Profiling in Wireless Network-on-Chip"
Brian Lebiednik, Sergi Abadal, Hyouk Jun Kwon and **Tushar Krishna**
Proc of 3rd International Workshop on Advanced Interconnect Solutions and Technologies for Emerging Computing Systems, Jan 2018
[Held in conjunction with the 13th HiPEAC Conference on High Performance Embedded Architectures and Compilers]

ICCAD 2017 "A Case for Low Frequency Single Cycle Multi Hop NoCs for Energy Efficiency and High Performance"
Monodeep Kar and **Tushar Krishna**
Proc of the IEEE/ACM International Conference on Computer-Aided Design, Nov 2017

NocArc 2017 "Lightweight Emulation of Virtual Channels using Swaps"
Mayank Parasar and **Tushar Krishna**
Proc of 10th International Workshop on Networks-on-Chip Architectures, Oct 2017
[Held in conjunction with the 50th Annual IEEE/ACM International Symposium on Microarchitecture (MICRO-50)]

NOCS 2017 "Rethinking NoCs for Spatial Neural Network Accelerators"
Hyoukjun Kwon, Ananda Samajdar, and **Tushar Krishna**
Proc of 11th International Symposium on Networks-on-Chip, Oct 2017

NOCS 2017 "Adaptive Manycore Architectures for Big Data Computing"
Janardhan Rao Doppa, Ryan Gary Kim, Mihailo Isakov, Michel A. Kinsy, Hyoukjun Kwon, and Tushar Krishna
Proc of 11th International Symposium on Networks-on-Chip, Oct 2017 (Special Session Paper)

ISPASS 2017 "OpenSMART: Single-Cycle Multi-hop NoC Generator in BSV and Chisel"
Hyoukjun Kwon and **Tushar Krishna**
Proc of the IEEE International Symp. on Performance Analysis of Systems and Software, Apr 2017

DATE 2017
Best Paper Award

"Automatic Place-and-Route of emerging LED-driven wires within a monolithically-integrated CMOS+III-V process"
Tushar Krishna, Arya Balachandran, Siau Ben Chiah, Li Zhang, Bing Wang, Cong Wang, Kenneth Lee Eng Kian, Jurgen Michel and Li-Shiuan Peh
Proc of Design Automation and Test in Europe, Mar 2017

HPCA 2017

"Static Bubble: A Framework for Deadlock-free Irregular On-chip Topologies"
Aniruddh Ramrakhyani and **Tushar Krishna**
Proc of the 23rd IEEE International Symp. on High-Performance Computer Architecture, Feb 2017

ISSCC 2016
Media Coverage:
IEEE Spectrum, Daily Mail, The Verge, phys.org, MIT News

"Eyeriss: An Energy-Efficient Reconfigurable Accelerator for Deep Convolutional Neural Networks"
Yu-Hsin Chen, **Tushar Krishna**, Joel Emer, and Vivienne Sze
Proc. of the IEEE International Solid-State Circuits Conference, Feb 2016

NOCS 2014
Best Paper Award

"Single-Cycle Collective Communication Over A Shared Network Fabric"
Tushar Krishna and Li-Shiuan Peh
Proc. of the 8th International Symposium on Networks-on-Chip, Sep 2014

Hot Chips 2014

"SCORPIO: A 36-Core Research Chip Demonstrating Snoopy Coherence on a Scalable Mesh NoC with In-Network Ordering"
Chia-Hsin Owen Chen, Sunghyun Park, Suvinay Subramanian, **Tushar Krishna**, Bhavya K. Daya, Woo-Cheol Kwon, Brett Wilkerson, John Arends, Anantha P. Chandrakasan, and Li-Shiuan Peh
Proc. of Hot Chips 26: A Symposium on High Performance Chips, Aug 2014

ISCA 2014
Media Coverage:
Wired, PC World, Geek, Phys, Tech, The Registrar, etc.

"SCORPIO: A 36-Core Research Chip Demonstrating Snoopy Coherence on a Scalable Mesh NoC with In-Network Ordering"
Bhavya K. Daya, Chia-Hsin Owen Chen, Suvinay Subramanian, Woo-Cheol Kwon, Sunghyun Park, **Tushar Krishna**, Jim Holt, Anantha P. Chandrakasan, and Li-Shiuan Peh
Proc. of the 41st International Symposium on Computer Architecture, Jun 2014

ASPLOS 2014

"Locality-Oblivious Cache Organization leveraging Single-Cycle Multi-Hop NoCs"
Woo-Cheol Kwon, **Tushar Krishna**, and Li-Shiuan Peh
Proc. of the 19th International Conference on Architectural Support for Programming Languages and Operating Systems, Mar 2014

DATE 2013

SMART: A Single-Cycle Reconfigurable NoC for SoC Applications"
Chia-Hsin Owen Chen, Sunghyun Park, **Tushar Krishna**, Suvinay Subramanian, Anantha P. Chandrakasan, and Li-Shiuan Peh
Proc. of Design Automation and Test in Europe, Mar 2013

HPCA 2013
Selected for IEEE Micro Top Picks

"Breaking the On-Chip Latency Barrier Using SMART"
Tushar Krishna, Chia-Hsin Owen Chen, Woo Cheol Kwon and Li-Shiuan Peh
Proc. of the 19th IEEE International Symp. on High-Performance Computer Architecture, Feb 2013

DAC 2012
Media Coverage:
EE Times, Slashdot, ACM, IT World, etc.

"Approaching the Theoretical Limits of a Mesh NoC with a 16-Node Chip Prototype in 45nm SOI"
Sunghyun Park, **Tushar Krishna**, Chia-Hsin Chen, Bhavya K. Daya, Anantha Chandrakasan, and Li-Shiuan Peh
Proc. of the 49th Design Automation Conference, Jun 2012

MICRO 2011 "Towards the Ideal On-chip Fabric for 1-to-Many and Many-to-1 Communication"
Tushar Krishna, Li-Shiuan Peh, Bradford M. Beckmann, and Steven K. Reinhardt
Proc. of the 44th IEEE/ACM International Symposium on Microarchitecture, Dec 2011

ICCAD 2011 "A Low-Swing Crossbar and Link Generator for Low-Power Networks-on-Chip"
Chia-Hsin Owen Chen, Sunghyun Park, **Tushar Krishna** and Li-Shiuan Peh
Proc. of the IEEE/ACM International Conference on Computer-Aided Design, Nov 2011

ICCD 2010 "SWIFT: A SWing-reduced Interconnect For a Token-based Network-on-Chip in 90 nm CMOS"
Tushar Krishna, Jacob Postman, Christopher Edmonds, Li-Shiuan Peh and Patrick Chiang,
Proc. of the 28th IEEE International Conference on Computer Design, Oct 2010

NOCS 2010 "Physical vs Virtual Express Topologies with Low-Swing Links for Future Many-core NoCs"
Chia-Hsin Owen Chen, Niket Agarwal, **Tushar Krishna**, Kyung-Hoae Koo, Li-Shiuan Peh and Krishna Saraswat
Proc. of the 4th International Symposium on Networks-on-Chip, May 2010

ISPASS 2009 "GARNET: A Detailed On-Chip Network Model inside a Full-System Simulator"
553 citations Niket Agarwal, **Tushar Krishna**, Li-Shiuan Peh and Niraj K. Jha
Proc. of the International Symp. on Performance Analysis of Systems and Software, April 2009

ICCAD 2008 "Texture Filter Memory – A Power-efficient and Scalable Texture Memory Architecture for Mobile Graphics Processors"
Silpa BVN, Anjul Patney, **Tushar Krishna**, Preeti R. Panda and G.S. Visweswaran
Proc. of the International Conference on Computer-Aided Design, Nov. 2008.

HotI 2008 "NoC with Near-Ideal Express Virtual Channels Using Global-Line Communication"
Selected for IEEE Micro Top Picks **Tushar Krishna**, Amit Kumar, Patrick Chiang, Mattan Erez, and Li-Shiuan Peh
Proc. of the 16th International Symposium on High-Performance Interconnects, Aug. 2008.

"Modeling Electron Transport Mechanism in a Molecular Diode through *ab initio* Molecular Energy Calculations"
Tushar Krishna, C Kiran, Dilip K. Maity and Swapan K Ghosh
Proc. of the DAE-BRNS Theme Meeting on Materials Modeling at Different Length Scales, BARC, Mumbai, India, 2006

PATENTS

"Message Broadcast with Router Bypassing"
Tushar Krishna, Bradford M. Beckmann, Steven K. Reinhardt.
US Patent 2011/0314255 A1, Issued: Dec 22, 2011

OPEN-SOURCE SOFTWARE RELEASES

Jan 2018 MAERI: An Open Source Framework for Generating Modular DNN Accelerators supporting Flexible Dataflow
http://synergy.ece.gatech.edu/tools/maeri/

May 2017 OpenSMART: A Tool for Automated Integration of Heterogeneous IPs
http://synergy.ece.gatech.edu/tools/opensmart

Oct 2016 Garnet2.0: An On-Chip Network Model for Heterogeneous SoCs
http://synergy.ece.gatech.edu/tools/garnet

TEACHING EXPERIENCE

Fall 2018 — **Georgia Tech ECE 3056 (Architecture, Concurrency and Energy in Computation)**
Undergraduate-level class of 90 students.

Spring 2018 — **Georgia Tech ECE 3056 (Architecture, Concurrency and Energy in Computation)**
Undergraduate-level class of 90 students.

Spring 2018 — **Georgia Tech GT ECE 8823 A / CS 8803 – ICN (Interconnection Networks)**
Graduate-level class of 26 students.

Summer 2017 — **Invited Lecturer for Network-on-Chip course at ACACES Summer School, Fuiggi, Italy**
Graduate-level class with 50+ registrants
The ACACES Summer School is a one-week summer school for computer architects and tool builders working in the field of high performance computer architecture and compilation for computing systems. It is organized by the High Performance and Embedded Architecture and Compilation (HiPEAC) consortium. The school aims at the dissemination of advanced scientific knowledge and the promotion of international contacts among scientists from academia and industry. It attracts PhD-students, faculty, and industry researchers.

Spring 2017 — **Georgia Tech ECE 8823 A / CS 8803 – ICN (Interconnection Networks)**
Graduate-level class of 11 students. *Teaching Score: 4.85/5*

Fall 2016 — **Georgia Tech ECE4100/ECE6100/CS4290/CS6290 (Advanced Computer Architecture)**
Graduate-level class of 62 students. *Teaching Score: 4.85/5*

Spring 2016 — **Georgia Tech ECE 8823 A / CS 8803 – ICN (Interconnection Networks)**
Graduate-level class of 21 students. *Teaching Score: 4.9/5*

Fall 2015 — **Georgia Tech ECE4100/ECE6100/CS4290/CS6290 (Advanced Computer Architecture)**
Graduate-level class of 39 students. *Teaching Score: 4.7/5*

TALKS

Sept 2017 — "Garnet2.0: A Detailed On-Chip Network Model inside a Full-System Simulator"
at *gem5 workshop, ARM Research Summit, Cambridge, U.K.*

Sept 2017 — "Breaking the On-Chip Latency Barrier Using Single-cycle Multi-hop Networks"
at *ARM Research, Cambridge, U.K.*

May 2017 — "Scalable and Low-Cost Heterogeneous Design in the Post-Moore's Law Era using Efficient Communication"
at *Georgia Tech ECE Advisory Board Meeting, Cupertino, CA, USA*

Apr 2017 — "Breaking the On-Chip Latency Barrier Using Single-cycle Multi-hop Networks"
at *Computer Engineering and Systems Group Seminar, Texas A&M University, TX, USA*

Feb 2017 — "Breaking the On-Chip Latency Barrier Using Single-cycle Multi-hop Networks"
at *Baidu Research, Sunnyvale, CA*

Oct 2016 — "Breaking the On-Chip Latency Barrier Using Single-cycle Multi-hop Networks"
at *Department of ECE, CALCM Seminar Series, Carnegie Mellon University, PA, USA*

Mar 2016 — "Breaking the On-Chip Latency Barrier Using SMART"
at *NVIDIA, Westford, MA, USA*

Mar 2015 — "Breaking the On-Chip Latency Barrier Using SMART"
at *Department of CS, University of California at Los Angeles, CA, USA*

Feb 2015 "Breaking the On-Chip Latency Barrier Using SMART"
at *Department of CS, University of Illinois Urbana-Champaign, IL, USA*

Feb 2015 "Breaking the On-Chip Latency Barrier Using SMART"
at *Department of ECE, Georgia Tech, Atlanta, GA, USA*

Jan 2015 "Enabling dedicated single-cycle connections over a shared multi-hop network"
at *Department of ECE, Northeastern University, Boston, MA, USA*

Nov 2014 "Enabling dedicated single-cycle connections over a shared Network-on-Chip"
at *Department of CSE, University of Michigan, Ann Arbor, MI, USA*

Sep 2014 "Single-Cycle Collective Communication Over A Shared Network Fabric"
at *IEEE Intl. Symp. on Networks-on-Chip (NOCS-8), Ferrara, Italy*

Feb 2013 "Breaking the On-Chip Latency Barrier Using SMART"
at *IEEE Intl. Symp. on High-Performance Computer Architecture (HPCA-19), Shenzhen, China*

Jul 2012 "Breaking the On-Chip Latency Barrier Using SMART"
at *VSSAD, Intel Corporation, Hudson, MA, USA*

May 2012 "Reconfigurable on-chip network topologies using SMART links"
at *Industry Affiliates Program, CSAIL, MIT, Cambridge, MA, USA*

Dec 2011 "Towards the Ideal On-chip Fabric for 1-to-Many and Many-to-1 Communication"
at *IEEE/ACM Intl. Symp. on Microarchitecture (MICRO-44), Porte Alegre, Brazil*

Oct 2010 "SWIFT: A SWing-reduced Interconnect For a Token-based Network-on-Chip in 90 nm CMOS"
at *IEEE Intl. Conf. on Computer Design (ICCD-28), Amsterdam, Netherlands*

Feb 2010 "SWing-reduced Interconnect For a Token-based (SWIFT) Network-on-Chip"
at *Student Research Preview, Intl. Solid-State Circuits Conference (ISSCC), San Francisco, CA*

Oct 2008 "NoC with Near-Ideal Express Virtual Channels Using Global-Line Communication"
at *Interconnect Focus Center (IFC) Annual Review, Atlanta, GA*

PROFESSIONAL SERVICE

Conference Organization:

- Co-Chair – 1st Rising Stars in Computer Architecture (RISC-A) Workshop 2018
- Publicity Co-Chair NOCS 2018
- Travel Grants Co-Chair PACT 2018
- Travel Grants Co-Chair ISCA 2017
- Workshops and Tutorials Chair ASPLOS 2016

Journal Reviewer:

- IEEE Journal on Emerging and Selected Topics in Circuits and Systems (JETCAS)
  - 2010
- IEEE Computer
  - 2013
- IEEE Computer Architecture Letters (CAL)
  - 2012, 2013, 2014, 2015, 2016, 2017, 2018
- ACM Transactions on Architecture and Code Optimization (TACO)
  - 2012, 2014, 2015, 2016, 2017
- IEEE Transactions on Very Large Scale Integration Systems (TVLSI)
  - 2014, 2016

- IEEE Transactions on Parallel and Distributed Systems (TPDS)
  - 2015
- IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)
  - 2016, 2017
- IEEE Transactions on Computers (TC)
  - 2016, 2018
- IEEE Transactions on Multi-Scale Computing Systems (TMCS)
  - 2017
- ACM Transactions on Embedded Computing Systems (TECS)
  - 2017

Conference External Review Committee (ERC) Member:

- IEEE/ACM International Symposium on Microarchitecture (MICRO)
  - 2015
- International Conference on Parallel Architectures and Compilation Techniques (PACT)
  - 2016
- IEEE International Symposium on Computer Architecture (ISCA)
  - 2017
- IEEE/ACM International Symposium on Microarchitecture (MICRO)
  - 2017
- IEEE International Symp. on High-Performance Computer Architecture (HPCA)
  - 2019
- ACM International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)
  - 2019

Program Committee Member:

- ACM/SIGARCH International Conference on Supercomputing (ICS)
  - 2015
- IEEE/ACM International Symposium on Microarchitecture (MICRO)
  - 2016, 2018
- Design Automation Conference (DAC)
  - 2016, 2017, 2018
- Design Automation and Test in Europe (DATE)
  - 2017, 2018, 2019
- IEEE International Symposium on High-Performance Interconnects
  - 2016, 2017
- IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS)
  - 2018
- IEEE International Parallel and Distributed Processing (IPDPS)
  - 2018

NSF Panels: 2016