

Tushar Krishna

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RESEARCH INTERESTS

Computer Architecture: multicore, parallel, heterogeneous, spatial, ML accelerators, FPGA

Interconnection Networks: Networks-on-Chip, HPC switches, data-centers, sensor networks

EDUCATION

Feb 2014 **Massachusetts Institute of Technology**

Ph.D. in Electrical Engineering and Computer Science

- *Advisor:* Prof. Li-Shiuan Peh
- *Committee:* Prof. Srinivas Devadas and Prof. Joel Emer
- *Thesis:* “Enabling Dedicated Single-Cycle Connections Over A Shared Network-on-Chip”

Sep 2009 **Princeton University**

M.S.E. in Electrical Engineering

- *Advisor:* Prof. Li-Shiuan Peh
- *Thesis:* “Networks-on-Chip with Hybrid Interconnects”

Aug 2007 **Indian Institute of Technology (IIT), Delhi**

B.Tech. (Honors) in Electrical Engineering

PROFESSIONAL EXPERIENCE

Aug '15 – present **Georgia Institute of Technology**, Atlanta, GA, USA

Assistant Professor

School of Electrical and Computer Engineering.

School of Computer Science (Adjunct).

Feb '15 – Jul '15 **Massachusetts Institute of Technology, SMART Center**, Cambridge, MA, USA

Post-doctoral Researcher.

Nov '13 – Jan '15 **Intel Corporation, VSSAD Group**, Hudson, MA

Research Engineer. Manager: Joel Emer

Jun'10 – Aug '10 **AMD (Advanced Micro Devices) Research**, Bellevue, WA, USA

Co-Op Engineer. Mentors: Bradford Beckmann and Steve Reinhardt

Jun'09 – Aug '09 **AMD Research**, Bellevue, WA, USA

Co-Op Engineer. Mentors: Bradford Beckmann and Steve Reinhardt

Jun'08 – Aug '08 **AMD**, North Bridge Architecture Group, Sunnyvale, CA, USA

Co-op Engineer. Mentor: Pat Conway

May'06 – Jul '06 **NVIDIA**, Digital Hardware Design Group, Bangalore, India

Summer Intern.

BOOKS

“On-Chip Networks”, Second Edition

Natalie Enright Jerger, **Tushar Krishna**, and Li-Shiuan Peh.

Synthesis Lectures on Computer Architecture. Morgan & Claypool Publishers. 2017

PUBLICATIONS (REFEREED JOURNALS)

- JSSC 2017** “Eyeriss: An Energy-Efficient Reconfigurable Accelerator for Deep Convolutional Neural Networks”
Yu-Hsin Chen, **Tushar Krishna**, Joel Emer, and Vivienne Sze
IEEE Journal of Solid State Circuits Conference, ISSCC Special Issue, Jan 2017
- TOCS 2015** “Efficient Control and Communication Paradigms for Coarse-Grained Spatial Architectures”
M. Pellauer, A. Parashar, M. Adler, B. Ahsan, R. Allmon, N. Crago, K. Fleming, M. Gambhir, A. Jaleel, **T. Krishna**, D. Lustig, S. Maresh, V. Pavlov, R. Rayess, A. Zhai, and J. Emer
ACM Transactions on Computer Systems, Sep 2015
- IEEE Micro Top Picks 2014** “SMART: Single-Cycle Multihop Traversals Over A Shared Network-on-Chip”
Tushar Krishna, Chia-Hsin Owen Chen, Woo-Cheol Kwon, and Li-Shiuan Peh
IEEE Micro (Special Issue: Top Picks from the Computer Architecture Conferences), May/June 2014
- IEEE Computer 2013** “Single-Cycle Multihop Asynchronous Repeated Traversal: A SMART Future for Reconfigurable On-Chip Networks”
Tushar Krishna, Chia-Hsin Owen Chen, Sunghyun Park, Woo-Cheol Kwon, Suvinay Subramanian, Anantha P. Chandrakasan, and Li-Shiuan Peh
IEEE Computer, 46(10): 48-55, Oct 2013
[Webex Chat with Guest Editor: \[youtu.be/k_I8yc_CjBU\]\(https://youtu.be/k_I8yc_CjBU\)](http://www.weebx.com/2013/08/20/ieee-computer-46-10-48-55-oct-2013/)
- TVLSI 2012** “SWIFT: A Low-Power Network-On-Chip Implementing the Token Flow Control Router Architecture With Swing-Reduced Interconnects”
Jacob Postman, **Tushar Krishna**, Christopher Edmonds, Li-Shiuan Peh, and Patrick Chiang
IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 21(8): 1432-1446, Aug 2012
- CAN 2011** “The gem5 simulator”
1639 citations N. Binkert, B. Beckmann, G. Black, S. K. Reinhardt, A. Saidi, A. Basu, J. Hestness, D. R. Hower, **T. Krishna**, S. Sardashti, R. Sen, K. Sewell, M. Shoaib, N. Vaish, M. D. Hill and D. A. Wood
SIGARCH Computer Architecture News, 39(2): 1-7, May 2011
- IEEE Micro Top Picks 2009** “Express Virtual Channels with Capacitively-Driven Global Links”
Tushar Krishna, Amit Kumar, Jacob Postman, Patrick Chiang, Mattan Erez, and Li-Shiuan Peh
IEEE Micro (Special Issue: Top Picks from Hot Interconnects 16), 29 (4): 48-61, Jul/Aug 2009

PUBLICATIONS (REFEREED CONFERENCES)

- ISPASS 2017** “OpenSMART: Single-Cycle Multi-hop NoC Generator in BSV and Chisel”
Hyoukjun Kwon and **Tushar Krishna**
Proc of the IEEE International Symp. on Performance Analysis of Systems and Software, Apr 2017
- DATE 2017** “Automatic Place-and-Route of emerging LED-driven wires within a monolithically-integrated CMOS+III-V process”
Best Paper Award **Tushar Krishna**, Arya Balachandran, Siau Ben Chiah, Li Zhang, Bing Wang, Cong Wang, Kenneth Lee Eng Kian, Jurgen Michel and Li-Shiuan Peh
Proc of Design Automation and Test in Europe, Mar 2017
- HPCA 2017** “Static Bubble: A Framework for Deadlock-free Irregular On-chip Topologies”
Aniruddh Ramrakhiani and **Tushar Krishna**
Proc of the 23rd IEEE International Symp. on High-Performance Computer Architecture, Feb 2017

- ISSCC 2016** “Eyeriss: An Energy-Efficient Reconfigurable Accelerator for Deep Convolutional Neural Networks”
Media Coverage: [IEEE Spectrum](#), [Daily Mail](#), [The Verge](#), [phys.org](#), [MIT News](#)
 Yu-Hsin Chen, **Tushar Krishna**, Joel Emer, and Vivienne Sze
Proc. of the IEEE International Solid-State Circuits Conference, Feb 2016
- NOCS 2014** “Single-Cycle Collective Communication Over A Shared Network Fabric”
Best Paper Award **Tushar Krishna** and Li-Shiuan Peh
Proc. of the 8th International Symposium on Networks-on-Chip, Sep 2014
- Hot Chips 2014** “SCORPIO: A 36-Core Research Chip Demonstrating Snoopy Coherence on a Scalable Mesh NoC with In-Network Ordering”
 Chia-Hsin Owen Chen, Sunghyun Park, Suvinay Subramanian, **Tushar Krishna**, Bhavya K. Daya, Woo-Cheol Kwon, Brett Wilkerson, John Arends, Anantha P. Chandrakasan, and Li-Shiuan Peh
Proc. of Hot Chips 26: A Symposium on High Performance Chips, Aug 2014
- ISCA 2014** “SCORPIO: A 36-Core Research Chip Demonstrating Snoopy Coherence on a Scalable Mesh NoC with In-Network Ordering”
Media Coverage: [Wired](#), [PC World](#), [Geek, Phys, Tech](#), [The Registrar](#), etc.
 Bhavya K. Daya, Chia-Hsin Owen Chen, Suvinay Subramanian, Woo-Cheol Kwon, Sunghyun Park, **Tushar Krishna**, Jim Holt, Anantha P. Chandrakasan, and Li-Shiuan Peh
Proc. of the 41st International Symposium on Computer Architecture, Jun 2014
- ASPLOS 2014** “Locality-Oblivious Cache Organization leveraging Single-Cycle Multi-Hop NoCs”
 Woo-Cheol Kwon, **Tushar Krishna**, and Li-Shiuan Peh
Proc. of the 19th International Conference on Architectural Support for Programming Languages and Operating Systems, Mar 2014
- DATE 2013** “SMART: A Single-Cycle Reconfigurable NoC for SoC Applications”
 Chia-Hsin Owen Chen, Sunghyun Park, **Tushar Krishna**, Suvinay Subramanian, Anantha P. Chandrakasan, and Li-Shiuan Peh
Proc. of Design Automation and Test in Europe, Mar 2013
- HPCA 2013** “Breaking the On-Chip Latency Barrier Using SMART”
Selected for IEEE Micro Top Picks **Tushar Krishna**, Chia-Hsin Owen Chen, Woo Cheol Kwon and Li-Shiuan Peh
Proc. of the 19th IEEE International Symp. on High-Performance Computer Architecture, Feb 2013
- DAC 2012** “Approaching the Theoretical Limits of a Mesh NoC with a 16-Node Chip Prototype in 45nm SOI”
Media Coverage: [EE Times](#), [Slashdot](#), [ACM](#), [IT World](#), etc.
 Sunghyun Park, **Tushar Krishna**, Chia-Hsin Chen, Bhavya K. Daya, Anantha Chandrakasan, and Li-Shiuan Peh
Proc. of the 49th Design Automation Conference, Jun 2012
- MICRO 2011** “Towards the Ideal On-chip Fabric for 1-to-Many and Many-to-1 Communication”
Tushar Krishna, Li-Shiuan Peh, Bradford M. Beckmann, and Steven K. Reinhardt
Proc. of the 44th IEEE/ACM International Symposium on Microarchitecture, Dec 2011
- ICCAD 2011** “A Low-Swing Crossbar and Link Generator for Low-Power Networks-on-Chip”
 Chia-Hsin Owen Chen, Sunghyun Park, **Tushar Krishna** and Li-Shiuan Peh
Proc. of the IEEE/ACM International Conference on Computer-Aided Design, Nov 2011
- ICCD 2010** “SWIFT: A SWing-reduced Interconnect For a Token-based Network-on-Chip in 90 nm CMOS”
Tushar Krishna, Jacob Postman, Christopher Edmonds, Li-Shiuan Peh and Patrick Chiang,
Proc. of the 28th IEEE International Conference on Computer Design, Oct 2010
- NOCS 2010** “Physical vs Virtual Express Topologies with Low-Swing Links for Future Many-core NoCs”
 Chia-Hsin Owen Chen, Niket Agarwal, **Tushar Krishna**, Kyung-Hoae Koo, Li-Shiuan Peh and Krishna Saraswat

Proc. of the 4th International Symposium on Networks-on-Chip, May 2010

- ISPASS 2009** “GARNET: A Detailed On-Chip Network Model inside a Full-System Simulator”
415 citations Niket Agarwal, **Tushar Krishna**, Li-Shiuan Peh and Niraj K. Jha
Proc. of the International Symp. on Performance Analysis of Systems and Software, April 2009
- ICCAD 2008** “Texture Filter Memory – A Power-efficient and Scalable Texture Memory Architecture for Mobile Graphics Processors”
Silpa BVN, Anjul Patney, **Tushar Krishna**, Preeti R. Panda and G.S. Visweswaran
Proc. of the International Conference on Computer-Aided Design, Nov. 2008.

- HotI 2008** “NoC with Near-Ideal Express Virtual Channels Using Global-Line Communication”
Selected for IEEE **Tushar Krishna**, Amit Kumar, Patrick Chiang, Mattan Erez, and Li-Shiuan Peh
Micro Top Picks *Proc. of the 16th International Symposium on High-Performance Interconnects, Aug. 2008.*

“Modeling Electron Transport Mechanism in a Molecular Diode through *ab initio* Molecular Energy Calculations”
Tushar Krishna, C Kiran, Dilip K. Maity and Swapan K Ghosh
Proc. of the DAE-BRNS Theme Meeting on Materials Modeling at Different Length Scales, BARC, Mumbai, India, 2006

PATENTS

“Message Broadcast with Router Bypassing”
Tushar Krishna, Bradford M. Beckmann, Steven K. Reinhardt.
US Patent 2011/0314255 A1, Issued: Dec 22, 2011

TEACHING EXPERIENCE

- Spring 2017** **Instructor for GT ECE 8823 A / CS 8803 – ICN (Interconnection Networks)**
Graduate-level class of 21 students.
- Fall 2016** **Instructor for GT ECE4100/ECE6100/CS4290/CS6290 (Advanced Computer Architecture)**
Graduate-level class of 62 students. *Teaching Score: 4.85/5*
- Spring 2016** **Instructor for GT ECE 8823 A / CS 8803 – ICN (Interconnection Networks)**
Graduate-level class of 21 students. *Teaching Score: 4.9/5*
- Fall 2015** **Instructor for GT ECE4100/ECE6100/CS4290/CS6290 (Advanced Computer Architecture)**
Graduate-level class of 39 students. *Teaching Score: 4.7/5*
- Fall 2011** **Teaching Assistant for MIT 6.823 (Computer System Architecture)**
Instructors: Prof. Arvind and Prof. Joel Emer
Graduate-level class of 24 students

TALKS

- Oct 2016 “Breaking the On-Chip Latency Barrier Using Single-cycle Multi-hop Networks”
at *Department of ECE, CALCM Seminar Series, Carnegie Mellon University, PA, USA*

- Mar 2016 “Breaking the On-Chip Latency Barrier Using SMART”
at *NVIDIA, Westford, MA, USA*

- Mar 2015 “Breaking the On-Chip Latency Barrier Using SMART”
at *Department of CS, University of California at Los Angeles, CA, USA*

- Feb 2015 “Breaking the On-Chip Latency Barrier Using SMART”
at *Department of CS, University of Illinois Urbana-Champaign, IL, USA*

- Feb 2015 “Breaking the On-Chip Latency Barrier Using SMART”
at *Department of ECE, Georgia Tech, Atlanta, GA, USA*

- Jan 2015 “Enabling dedicated single-cycle connections over a shared multi-hop network”
at *Department of ECE, Northeastern University, Boston, MA, USA*

- Nov 2014 “Enabling dedicated single-cycle connections over a shared Network-on-Chip”
at *Department of CSE, University of Michigan, Ann Arbor, MI, USA*

- Sep 2014 “Single-Cycle Collective Communication Over A Shared Network Fabric”
at *IEEE Intl. Symp. on Networks-on-Chip (NOCS-8), Ferrara, Italy*

- Feb 2013 “Breaking the On-Chip Latency Barrier Using SMART”
at *IEEE Intl. Symp. on High-Performance Computer Architecture (HPCA-19), Shenzhen, China*

- Jul 2012 “Breaking the On-Chip Latency Barrier Using SMART”
at *VSSAD, Intel Corporation, Hudson, MA, USA*

- May 2012 “Reconfigurable on-chip network topologies using SMART links”
at *Industry Affiliates Program, CSAIL, MIT, Cambridge, MA, USA*

- Dec 2011 “Towards the Ideal On-chip Fabric for 1-to-Many and Many-to-1 Communication”
at *IEEE/ACM Intl. Symp. on Microarchitecture (MICRO-44), Porte Alegre, Brazil*

- Oct 2010 “SWIFT: A SWing-reduced Interconnect For a Token-based Network-on-Chip in 90 nm CMOS”
at *IEEE Intl. Conf. on Computer Design (ICCD-28), Amsterdam, Netherlands*

- Feb 2010 “SWing-reduced Interconnect For a Token-based (SWIFT) Network-on-Chip”
at *Student Research Preview, Intl. Solid-State Circuits Conference (ISSCC), San Francisco, CA*

- Oct 2008 “NoC with Near-Ideal Express Virtual Channels Using Global-Line Communication”
at *Interconnect Focus Center (IFC) Annual Review, Atlanta, GA*

HONORS AND AWARDS

- 2017 **Best Paper Award** (Design Methods and Tools Track) at Design Automation and Test in Europe (DATE)
 - 2014 **Best Paper Award** at the 8th International Symposium on Networks-on-Chip (NOCS)
 - 2009 **IEEE Micro Top Picks** from Computer Architecture Conferences
 - 2007-08 **IEEE Micro Top Picks** from Hot Interconnects
 - 2007 **Princeton Graduate Fellowship**
 - 2004-2006 ICIM Stay Ahead Award for the **Best Undergraduate Project in Computer Technology**, IIT Delhi
“National Initiative for Undergraduate Sciences” (NIUS) Fellowship, Homi Bhabha Centre for Science
Education (HBCSE), India
 - 2003, 2004 Merit prize for academic excellence, IIT Delhi
 - 2003 **Gold Medal** at the Indian National Chemistry Olympiad – one of top 25 Indians
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PROFESSIONAL SERVICE

External Reviewer: JETCAS 2010, NOCS 2011, CAL 2012, TACO 2012, IEEE Computer 2013, CAL 2013, TVLSI 2014, TACO 2014, CAL 2014, CAL 2015, TPDS 2015, TACO 2015, MICRO 2015, ICECS 2015, TVLSI 2016, TCAD 2016, CAL 2016, Trans. Computers 2016

Program Committee: ICS 2015, PACT (ERC) 2016, DAC 2016, MICRO 2016, Hot Interconnects 2016, DATE 2017, ISCA (ERC) 2017, DAC 2017

NSF Panels: 2016

Conference Organization:

- Workshops and Tutorials Chair ASPLOS 2016
- Travel Grants Co-Chair ISCA 2017

REFERENCES

Upon request
