

**The
Propagation
Group**

**Design and Construction of a
GHz Sliding Correlator Channel
Sounder for Wireless Channel
Characterization and Analysis**

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Undergraduate Research Project:

Design and Construction of a Gigahertz Sliding Correlator Channel
Sounder for Wireless Channel Characterization and Analysis

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Introduction

Wireless systems have become a dominant presence in our lives. From voice communication to data transmission and general connectivity, wireless options existed that allow greater mobility and freedom than their wired counterparts. As more time and money was invested in the wireless industry, products began to show up on the market ranging from cell phones to wireless LAN devices to ad hoc Bluetooth type devices. With the growing need for more bandwidth and increased data rates, in combination with the saturation of existing wireless channels, the FCC is considering opening new spectrums centered at several tens of Gigahertz. While technology has allowed us to push the envelopes of the frequency spectrum and utilize ever-increasing frequencies for communication, our understanding of the propagation characteristics of such high frequency channels has lagged behind.

The task proposed for this undergraduate research project was the design and construction of a Gigahertz sliding correlator channel sounder, an instrument used for the characterization and analysis of wireless channels [1]. This project greatly mirrors the work done by Chris R. Anderson as detailed in his Master's thesis, which has served as an excellent reference for much of the information in this document [1].

The Multipath Problem

At very low frequencies, wireless transmission may approach the textbook concept of transmitting and receiving a single signal [1]. However, as clock rates go up, so does the complexity of wireless transmission. Electromagnetic waves reflect, diffract, and scatter, alleviating the need for direct line of sight between transmitter and receiver, but also creating the complicated multipath problem. Multipath is the nearly infinite number of paths that a signal can take from transmitter to receiver, reflecting off smooth objects, scattering off rough objects, and diffracting around sharp corners [1]. When a high frequency signal is transmitted, it is received not once, but several times at the receiver. Signals that bounce around in the environment and have longer overall path lengths take a longer to reach the receiver. The more the signal bounces off and around objects along a given path, the longer it takes to reach the receiver and, generally speaking, the more it is attenuated.

Introduction to Spread Spectrum

The channel sounder works by sending a broadband signal over a given channel using a technique called "spread spectrum" [1]. Spread spectrum originated as a means of secure communication for the military, spreading a signal out in the frequency domain to give it a very low peak power. To observers, a spread spectrum signal looks similar to white noise, and thus has a Low Probability of Intercept (LPI). The noise-like properties of a spread spectrum signal are achieved by modulating the signal with a pseudo-random noise (PN) code, which is a pseudo-random binary sequence. PN codes are generated by shift registers configured with linear feedback taps, and this will be detailed in a later section. The PN code exhibits some interesting properties, which will be noted for the sake of completeness.

- 1) The Maximal Length Linear Shift Register (MLSR) sequence has a period of L chips, with $L = 2^N - 1$. (That is, an N bit shift register can generate a PN code of L bits, where the maximum value of L is $2^N - 1$.)

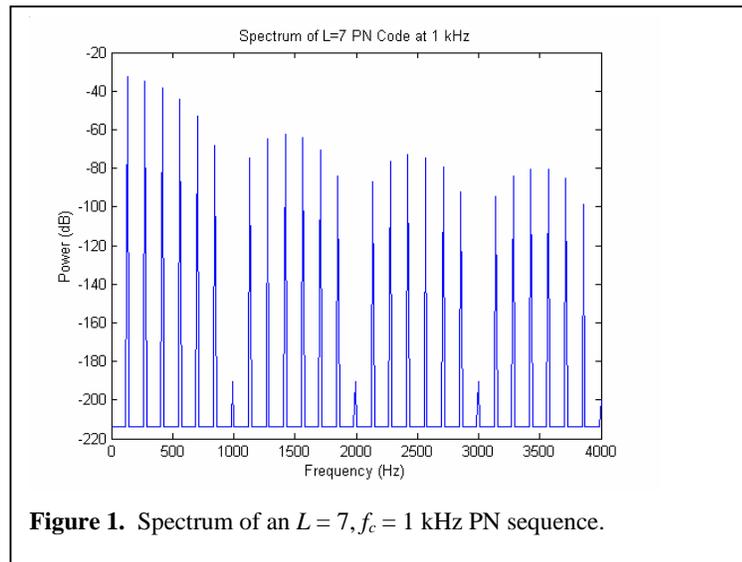
- 2) The statistical distribution of “1’s” and “0’s” is the same as in a random sequence with the exception that the total number of “1’s” is always one larger than the total number of “0’s”, independent of the length of the code. (Note that this implies only codes of odd length are possible.)
- 3) The modula-2 sum of any m-sequence with a shifted version of itself produces another shifted version of the same sequence.
- 4) All possible N -bit words will appear in the sequence exactly once, except for the all-zeros combination. (The all-zeros combination should never occur because the shift register will become locked in this state.)
- 5) The autocorrelation of the PN sequence is given by $R_{xx}(\tau)$:

$$R_{xx}(\tau) = -\frac{1}{L} \sum_{\ell=-\infty}^{\ell=\infty} \left(1 + \frac{1}{L}\right) \Delta\left(\frac{\tau - \ell T_c}{T_c}\right)$$

T_c is the clock rate (also known as the chip rate)

$$\Delta\left(\frac{t}{\tau}\right) = \begin{cases} 1 - \frac{|t|}{\tau}, & |t| \leq T_c \\ 0, & |t| > T_c \end{cases}$$

The spectrum of the PN code follows a $\text{sinc}^2(f)$ envelope, with the nulls occurring at integral multiples of the clock frequency [1]. The spectrum is made up of discrete peaks between envelope nulls. The number of peaks between nulls is given by $L - 1$ where L is the length of the PN sequence. Figures 1 and 2 show the spectrum and autocorrelation of the PN code.



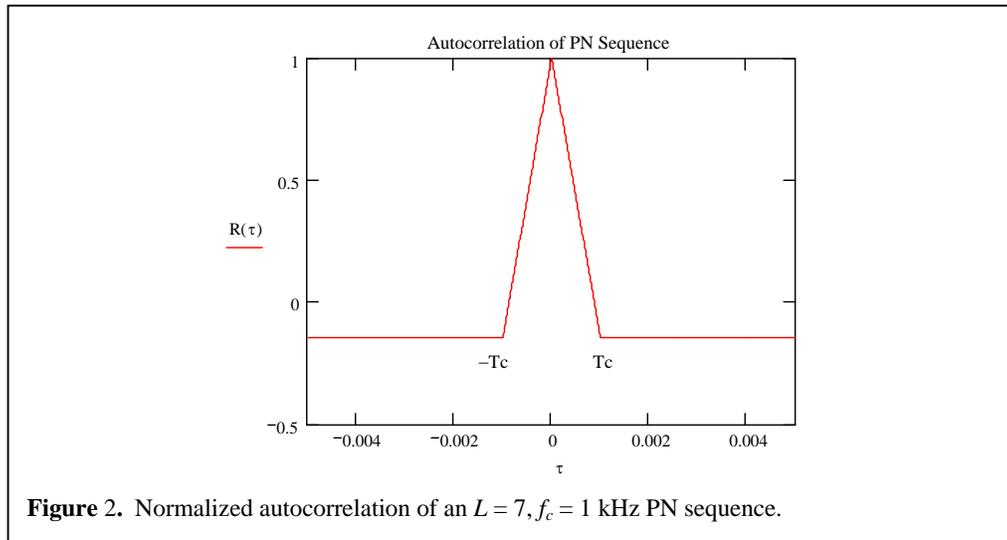


Figure 2. Normalized autocorrelation of an $L = 7, f_c = 1$ kHz PN sequence.

Channel Sounder Fundamentals

The sliding correlator channel sounder clocks the PN codes at very high frequencies to fill a wireless channel with noise-like content [1]. The PN codes are modulated onto the carrier frequency and transmitted across the channel. Some distance away, a receiver demodulates the signal and performs the “sliding correlation”. The received PN code, which is clocked by the transmitter at some frequency f_T , is mixed with an identical PN code clocked by the receiver at some slightly slower frequency f_R . Because the received PN code is clocked at a higher frequency than the PN code generated at the receiver, the received code slides past the slower receiver-generated code in time.

When the faster code slides past the slower code such that they are momentarily perfectly aligned, the crosscorrelation will be very large. At points of poor alignment, the crosscorrelation will be $-1/N$. This was indicated by the autocorrelation of the PN code. A series of alignments due to the multipath environment will generate a series of triangular peaks in the crosscorrelation. This effectively is the impulse response of the channel. By taking the Fourier Transform of this impulse response, the frequency response of the channel may be found.

PN Generator Overview

The PN generator is based around a shift register configured with linear feedback [2]. Certain registers on the shift register are selected as feedback taps. The bits at these taps are XOR-ed together (modulo-2 addition). The output of the modulo-2 addition is sent to the input of the shift register. This configuration is the Fibonacci architecture for a linear feedback shift register [3]. Another configuration, called the Galios architecture, is functionally equivalent but performs operations in parallel, rather than in series. The Galois PN generator is generally faster than the Fibonacci PN generator due to its parallel architecture. Figure 3 compares a Galois and Fibonacci implementation.

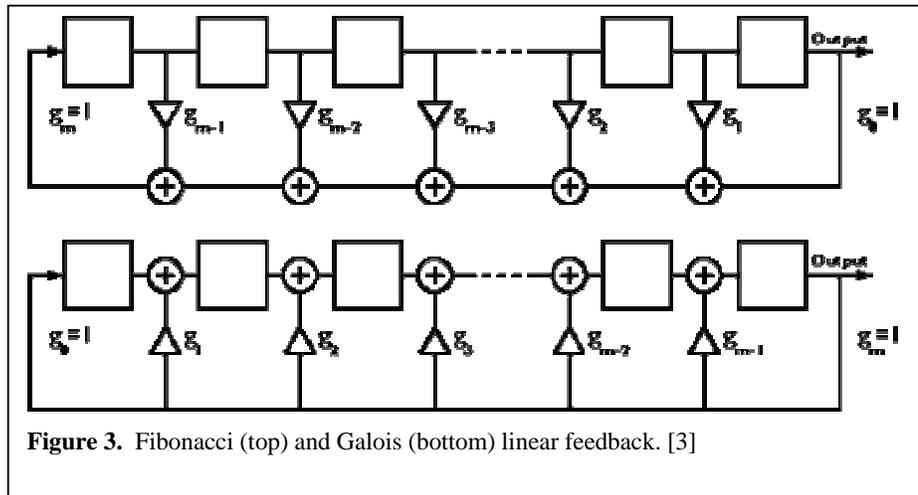


Figure 3. Fibonacci (top) and Galois (bottom) linear feedback. [3]

Note that the Galois architecture requires parallel I/O for the shift register, while the Fibonacci implementation requires shift in / parallel out for the shift register. One other item of interest is that the “output” of a PN generator can be taken from basically anywhere in the circuit. All registers and XOR gates will output the same PN code, though they will all be out of phase from each other.

Selecting the correct registers to use as feedback taps is an important in designing the PN generator. Only certain feedback configurations give rise to what is called a maximal-length sequence, or m-sequence for short. M-sequences are the longest possible codes that a PN generator can produce before repeating. For an N-bit shift register, its m-sequence length is given by L in the Equation 1.

$$L = 2^N - 1 \quad (\text{Eq. 1})$$

All other feedback tap configurations will result in a sequence length that is less than L. Therefore, to make the best use of the shift register, it is important to choose feedback taps that give rise to an m-sequence. This is not a difficult task, as data tables abound that provide the proper feedback taps for a given shift register size [3]

In order to begin outputting the PN code, the shift register must be initialized to some non-zero value. Typically, the shift register is filled with 1’s via the use of an OR gate between the final XOR gate and the shift register [2]. One of the OR gate inputs is the XOR gate output. The other OR gate input is used to switch the PN generator between initialization mode and normal operation. A diagram of this setup is shown in Figure 4.

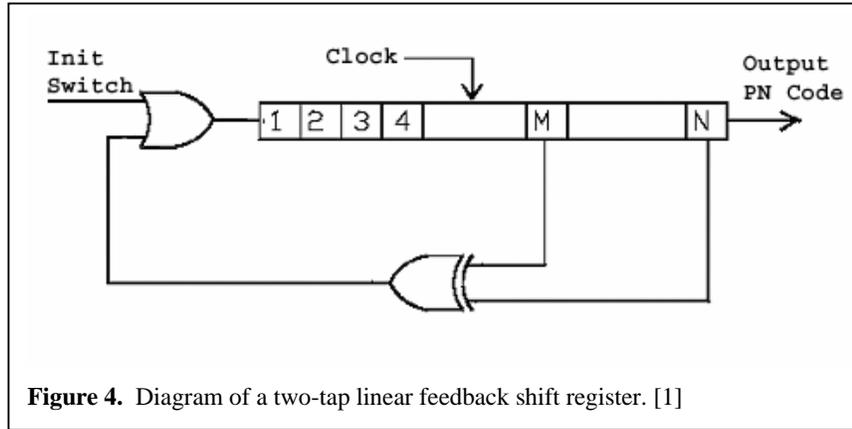


Figure 4. Diagram of a two-tap linear feedback shift register. [1]

PN Generator Design Choices

There are two principle variables that had to be determined before design could begin. These were the clock frequency f_c of the PN generator and the size of the shift register N . The choice for these variables has a tremendous effect on the performance of the sliding correlator channel sounder, as is indicated in Table 1.

Table 1. System Parameter Dependencies [1]

System Parameter	PN Generator Property	Dependence
Time Domain Resolution of Multipath Signals	Clock frequency, f_c	$T_{Res} = \frac{1}{f_c}$ (sec)
Dynamic Range	Code length, L_{PN}	$D_R = 20\log(L_{PN})$ (dB)
Maximum Resolvable Multipath Delay Time	Code length and Clock frequency	$T_{Max} = \frac{L_{PN}}{f_c}$ (sec)
Process Gain	Slide factor, k , and Clock frequency	$G_P = 10\log\left(\frac{0.88f_c}{k}\right)$ (dB)
Maximum Doppler Shift Resolution	Slide factor, Clock frequency, and Code length	$f_{D_{MAX}} = \frac{f_c}{2kL_{PN}}$ (Hz)
RF Bandwidth	Clock frequency	$BW = 2f_c$ (Hz)

Many of the system parameters are beyond the current scope of this project. However, the dynamic range and RF bandwidth can be addressed here. The dynamic range is related to the peak value of the autocorrelation and thereby, the length of the sequence. When a longer sequence is autocorrelated, its peak value will be greater than that of a shorter sequence. Greater dynamic range allows for more accurate analysis of the channel and a greater SNR of the output impulse response.

The RF bandwidth refers is directly related to the clock frequency. The sliding correlator channel needs to produce a wide band signal to determine the frequency response of the wireless channel. Therefore, the PN generator must be clocked at a very high frequency. Recall that the PN code spectra resembles $\text{sinc}^2(f)$ with nulls

occurring at the integer multiples of the clock frequency. The RF bandwidth is a measure of the size of the main hump in the envelope, as much of the spectral power is in the range of $\pm f_c$. Thus, the faster the PN generator is clocked, the larger the bandwidth of the signal. It is desired to sound the channel with signals that have a bandwidth of 1 GHz or more, so the PN generator must be able to operate at extremely high frequencies. Clocking at these frequencies requires a special family of integrated circuits called Emitter-Coupled Logic (ECL).

Circuit Design

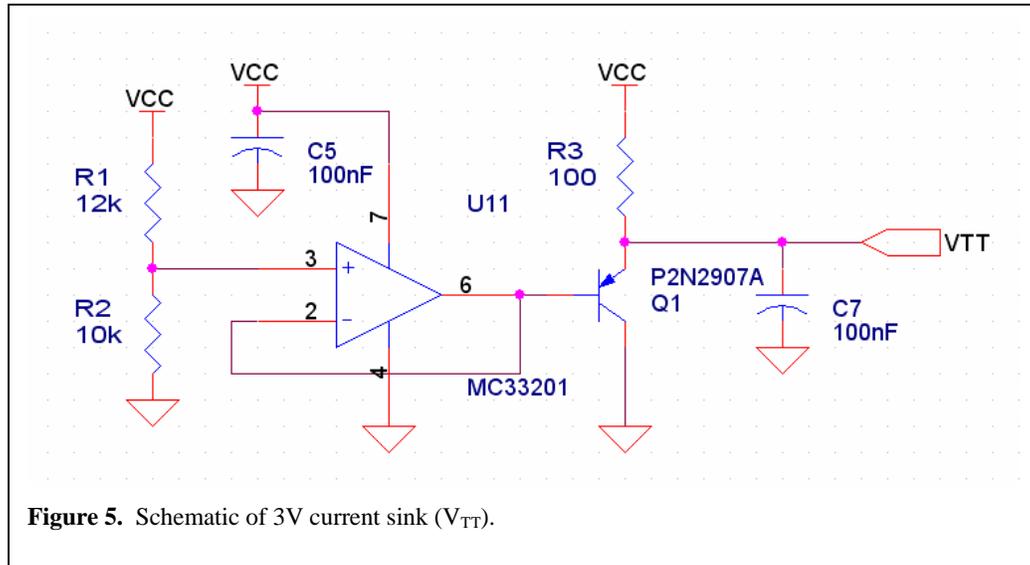
The PN generator was designed using ECL devices. There were five main components of the PN generator design: the 3 Volt sink, the shift register clock, the bias voltage, the initialization circuit, and the linear feedback shift register (LFSR).

3 Volt Current Sink

It was mentioned earlier that the Thevenin equivalent termination scheme seemed to be the preferred method, but for some reason this scheme had implementation problems that resulted in the destruction of several devices. Therefore, after much difficulty, the 3 V supply scheme was chosen. However, this presented another problem, because with the exception of the ground terminal, most power supply terminals do not sink current very well. Tests showed that voltage would build up on the 3 V supply terminal if one tried to sink too much current into the terminal, leading to an actual voltage greater than 3 V. To resolve this problem, it was found that by connecting a resistor from the 3 V terminal to ground allowed the power supply to divert any current going into the 3 V terminal to ground. The value of this resistor should be chosen so that the current from 3 V to ground is always equal to or greater than the current being sunk into 3 V.

Of course, this is not a very elegant scheme, and still requires an extra supply. To avoid this, a 3 Volt sink was designed using an op-amp and a PNP transistor. The op-amp was configured as a voltage-follower to produce 2.3 V at the base of the transistor. The transistor was operated in the forward-active region to ensure approximately a 0.7 V drop from the emitter to the base. By grounding the collector terminal, the voltage drop from emitter to collector was approximately 3.0 V. Looking into the transistor from the emitter, the transistor has a very low impedance and thereby acts as an excellent current sink.

To generate the 2.3 V at the op-amp output, a simple voltage divider was used. The actual voltage generated by the voltage divider was 2.27 V. However this was acceptable, as it was better for the 3 Volt sink to be a slightly less than 3 V rather than greater. This would mean that the ECL outputs would source slightly more current than nominal, but also makes it less likely for V_{TT} to ever be greater than V_{OL} . Another caveat of the current sink was that, in order for the transistor to operate in the forward-active region and thereby have $V_{EB} = 0.7$ V, the transistor had to sink at least 20 mA of current. When an ECL output is low, it sources $0.25/50 = 5$ mA, and when high, $1.05/50 = 21$ mA. Obviously it is not difficult to meet this requirement simply by connecting devices to the current sink. However, to ensure that the 3 Volt sink is always approximately 3 Volts, a 100 ohm resistor to V_{CC} was used to sink 20 mA of current into the transistor's emitter. The final 3V current sink circuit is shown in Figure 5.



When implementing this sink, there were several other considerations. For one, all the current entering the emitter will be divided between the collector and the base, with the majority going to the collector as defined by $i_E = i_C + i_B = (\beta + 1) i_B$ where β is the current gain for the transistor. This means that a very small amount of current will go through the op-amp to ground, and it is important to ensure that the amount of current is within the op-amp's current sinking limits. The op-amp used in the circuit, which was an MC33201 could sink or source up to 80 mA. Also, the transistor used here, which was a P2N2907A, can sink at most 600 mA of current. If we assume all ECL outputs connected to this sink are high and generously estimate an output high current of 30 mA (corresponding to $V_{OH} = 4.5$ V), taking into account the 20 mA provided by the pull-down resistor the current sink can support at most $(600 \text{ mA} - 20 \text{ mA}) / (30 \text{ mA}) = 19.3$, or 19 ECL outputs. Even with a current gain as low $\beta = 50$ the base current is only 12 mA, well within the specifications of the op-amp.

Shift Register Clock

The shift register clock was designed around the MC10EP16 differential receiver. This chip has a V_{BB} pin to be connected to the unused input of its differential input, as described in an earlier section. This proved to be the only V_{BB} source available in the overall design, so this pin was connected to an op-amp configured as a voltage-follower. This provided a steady V_{BB} source that could be connected to other chips where a single-ended output was connected to a differential input. Additionally this alleviated the need to consider how much current the V_{BB} pin was actually sourcing. Note that the V_{BB} pin was not an actual ECL output and thus did not require current sourcing to reach the proper voltage level.

The circuit shown in Figure 6 was used to bias an 800mV_{p-p} 0V_{DC} square wave to the proper voltage levels required by the ECL devices. Early biasing circuits used V_{BB} to bring the input clock up to proper voltage levels. However, this coupled the clocks noisy signal onto V_{BB} . It was therefore decided to bias the clock using a voltage divider circuit that generated an approximation of V_{BB} .

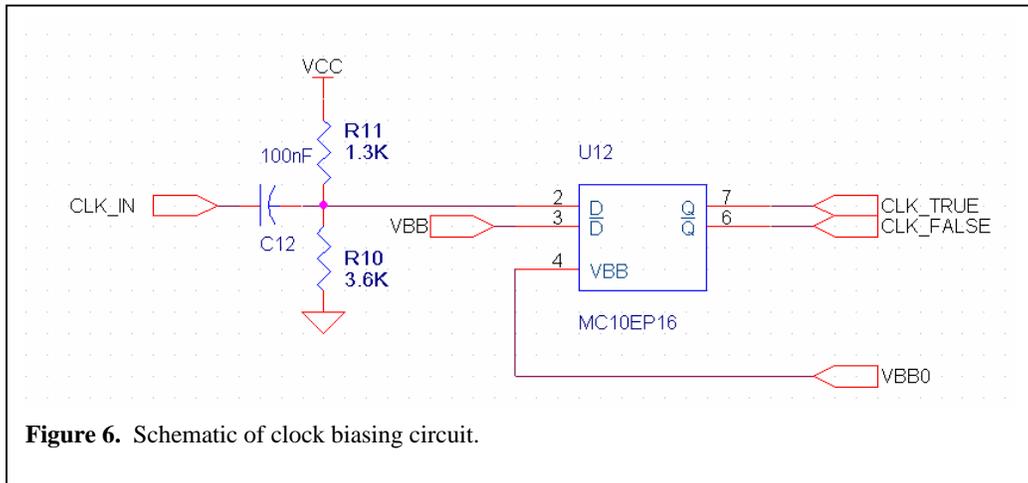


Figure 6. Schematic of clock biasing circuit.

An $800\text{ mV}_{\text{p-p}}$, 0 V_{DC} square wave is fed into the circuit via the capacitor. The capacitor serves as a DC block but allows the square wave to pass. The two resistors generate an approximation of V_{BB} , pulling the clock signal up to proper ECL voltage levels. This is then fed into the true input of the MC10EP16. The inverted input is tied to a buffered V_{BB} . According to the specifications for an ECL differential input, the input will be high when the true input is greater than the inverted, and the input will be low for the reverse case. The MC10EP16 essentially acts as a high-speed buffer.

Bias Voltage (V_{BB})

The ECL bias voltage, V_{BB} , was generated by an op-amp configured as a voltage-follower. The reference voltage was V_{BB0} generated by the MC10EP16 driver. Capacitors decouple V_{BB0} and V_{CC} . The bias voltage circuit is shown in Figure 7.

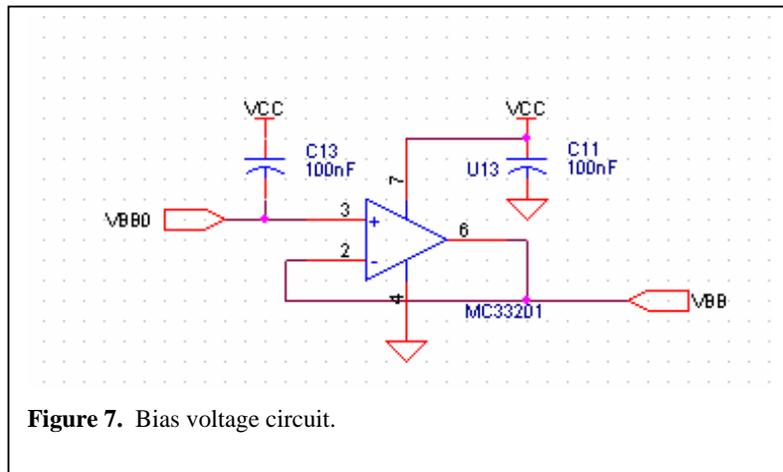


Figure 7. Bias voltage circuit.

Initialization Circuit

The initialization circuit shown in Figure 8 was used to set the output of the OR gate high. This caused the shift register to fill with binary ‘1’s and initialized the PN sequence. A voltage divider was used to generate approximately 4.05 V. When the

switch is pressed, PN_INIT goes high. When the switch is released, PN_INIT floats low, because it is connected to an input of the OR gate that defaults to '0' when open.

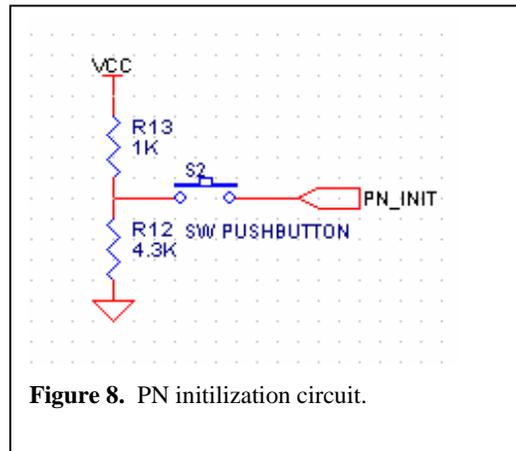


Figure 8. PN initialization circuit.

Linear Feedback Shift Register

The linear feedback shift register (LFSR) circuitry shown in Figure 9 consists of three ICs: the MC10EP142 9-bit shift register, the MC10EP08 differential XOR gate, and the MC10EP01, a single-ended quad-input OR gate. When properly configured, the LFSR's maximal length sequence is $2^9 - 1 = 511$ bits. To generate this sequence, the outputs of registers 5 and 9 were connected to the two true inputs of the XOR gate. The inverted inputs were tied to the buffered VBB.

The true output of the XOR's differential output was connected to one of the OR gate's input pins. Another one of the OR gate's input pins was connected to a switch that when pressed, provided V_{OH} at the pin via a voltage divider. When the switch was open the pin would be unconnected, and according to the specifications of the MC10EP01, all unused pins would default to V_{OL} . The OR gate and switch act as an initialization circuit for the LFSR.

The differential output of the OR gate was connected to the differential S-IN input on the shift register, thereby completing the feedback loop. The differential output of the MC10EP16 was connected to both differential clocks on the shift register. This was necessary in order for the shift register to function properly. Finally, the SEL pin was pulled high via a voltage divider so as to set the shift register in "shift mode". Refer to the data sheets for additional information concerning each device.

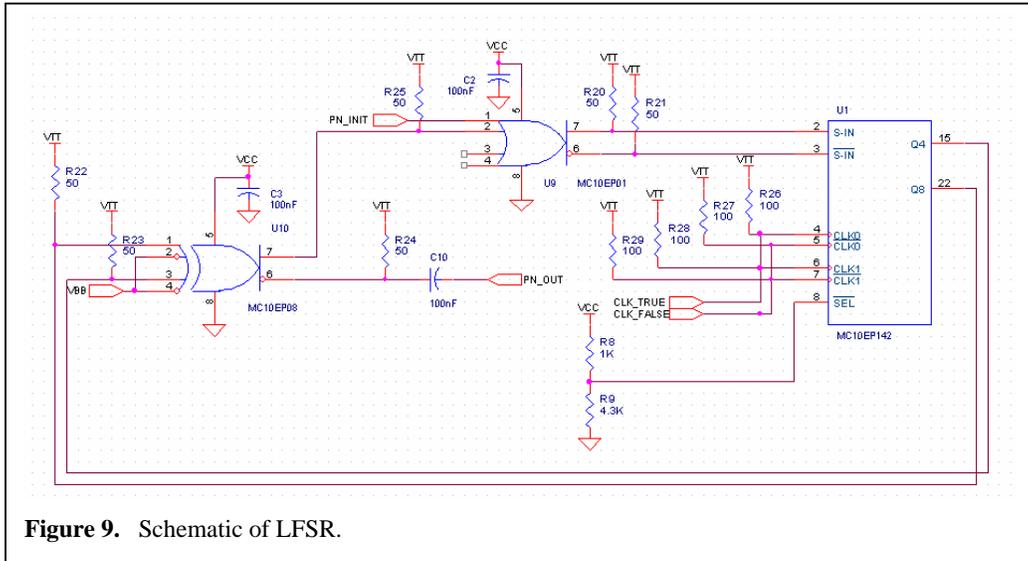


Figure 9. Schematic of LFSR.

Implementation

The circuit was designed, built, and tested on a protoboard before beginning a PCB layout of the circuitry. The protoboard implementation achieved a maximum clock frequency of 30 MHz. Figure 10 shows the protoboard implementation PN generator clocked at 1 MHz as well as the expected sinc-squared output.

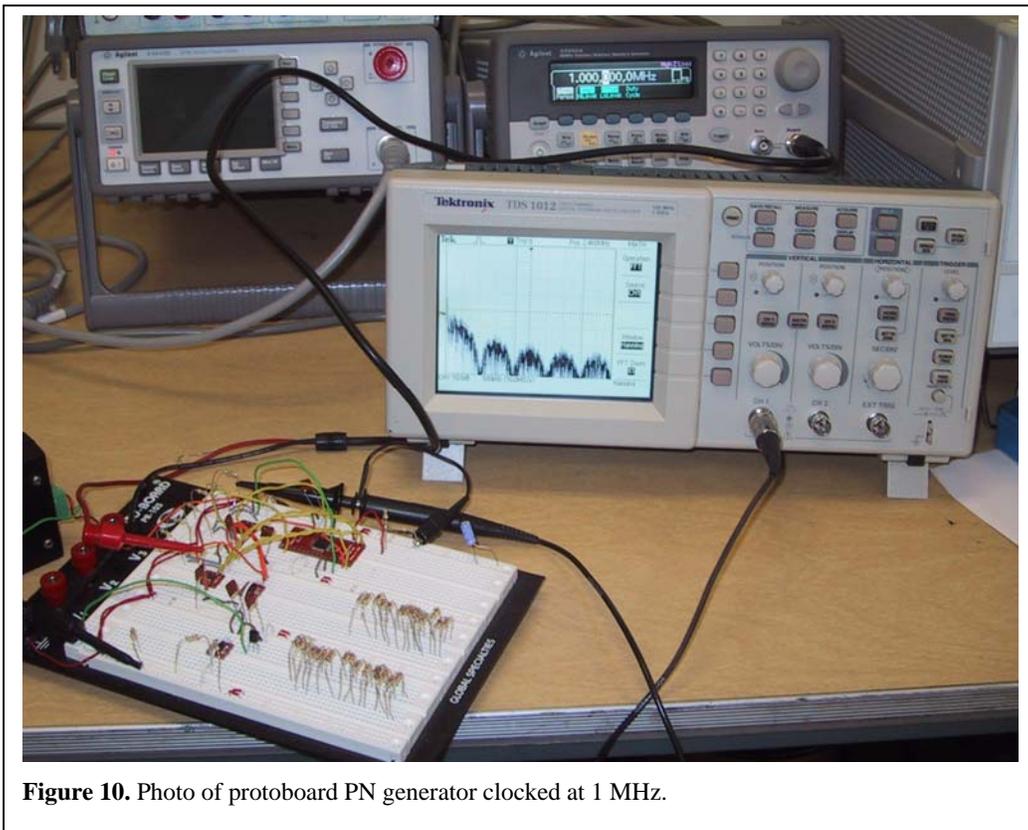


Figure 10. Photo of protoboard PN generator clocked at 1 MHz.

This satisfactory performance indicated the PN generator was ready to be implemented on a printed circuit board (PCB). Layout was performed in Cadence

Layout Plus. The board's dimensions were 3 in. by 3 in. The layout is illustrated in Figure 11. Two such boards were manufactured. Figure 12 shows the fully assembled PN generator.

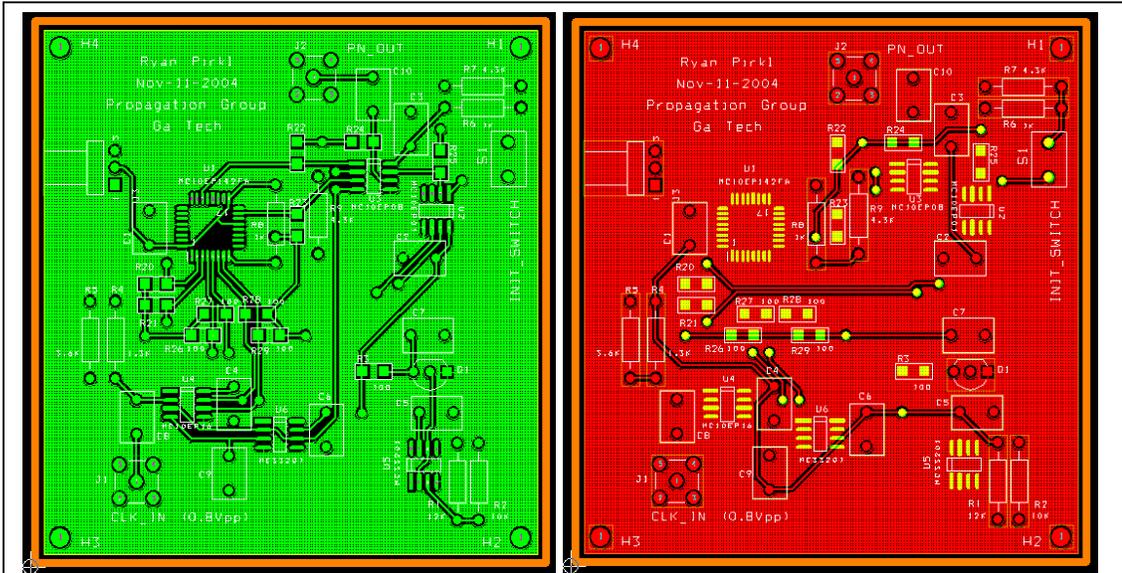


Figure 11. Board layout for top (left) and bottom (right).

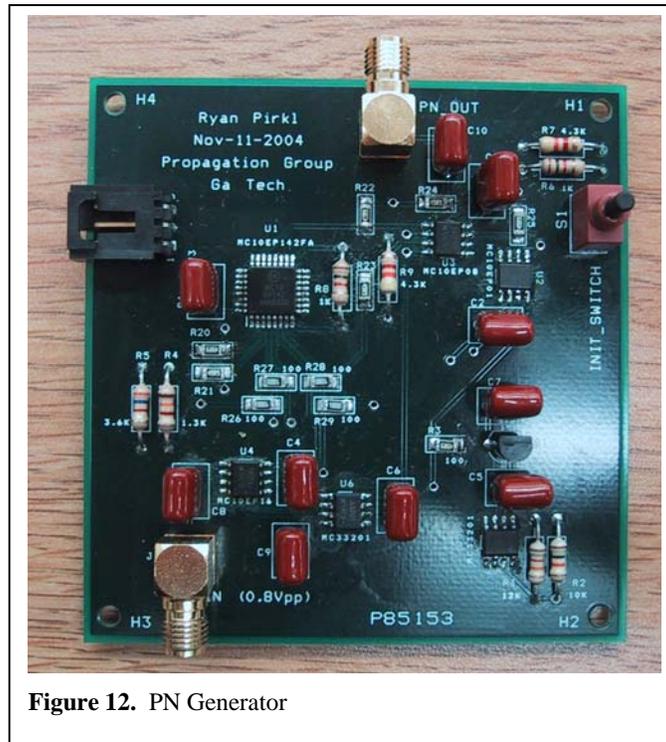


Figure 12. PN Generator

These boards served as prototypes for continued analysis of the system. They achieved a maximum clock frequency of 460 MHz, though at this frequency, the sinc-

squared envelope was considerably degraded as compared to the envelope generated by a 300 MHz clock, as shown in Figure 13.

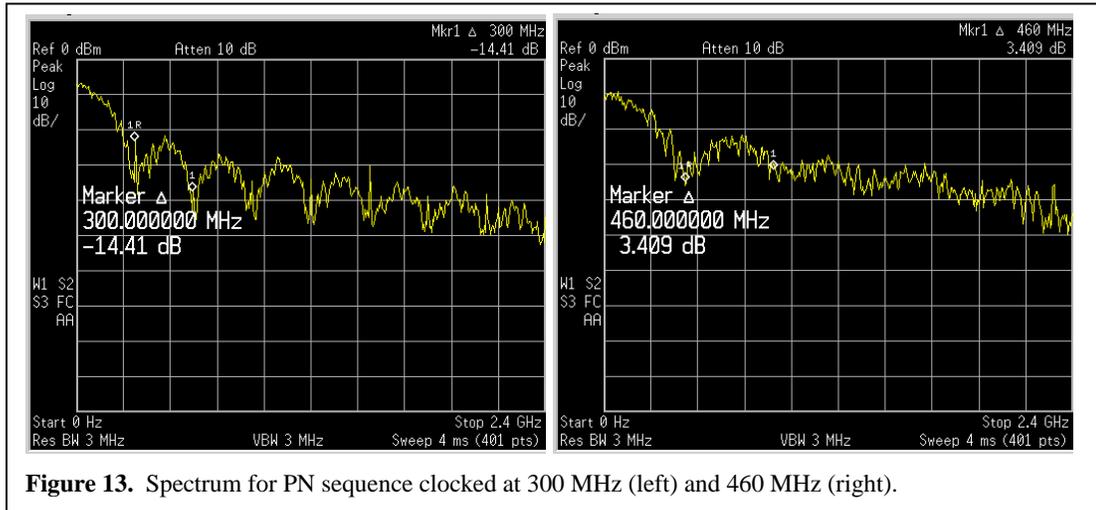


Figure 13. Spectrum for PN sequence clocked at 300 MHz (left) and 460 MHz (right).

Figure 14 indicates that the PN generator is producing the correct PN sequence for 300 MHz and 460 MHz. Recall that there should be $L - 1 = (2^9 - 1) - 1 = 510$ peaks between envelope nulls. At 300 MHz, there is 600 kHz between peaks. $(600 \text{ kHz}) / (300 \text{ MHz}) = 500$ peaks. At 460 MHz, there is 900 kHz between peaks. $(900 \text{ kHz}) / (460 \text{ MHz}) = 511.1$ peaks. Taking into account measurement error, this is a good indication that the PN sequence is correct.

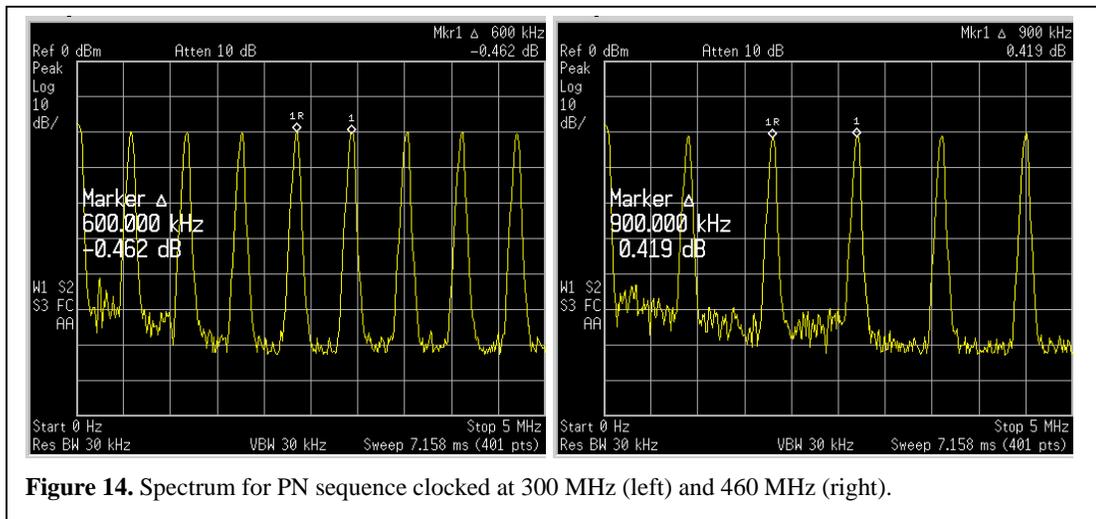


Figure 14. Spectrum for PN sequence clocked at 300 MHz (left) and 460 MHz (right).

Future Design Considerations

This first generation PCB was a single-layer board made of FR-4. A 50-ohm trace on single-layer FR-4 with thickness 0.062 in. must be 0.066 in. wide. The traces on this board were 0.012 in. wide, as such a wide trace was not practical. The traces had an impedance of 85-ohms, making impedance mismatches significant. In attempt to minimize the reflections, the traces were made as short as possible. The longest trace on the board had a length of roughly 2.2 in. Therefore, transmission line effects would become significant for a wavelength of 22 in. or 0.5588 meters. The traces had

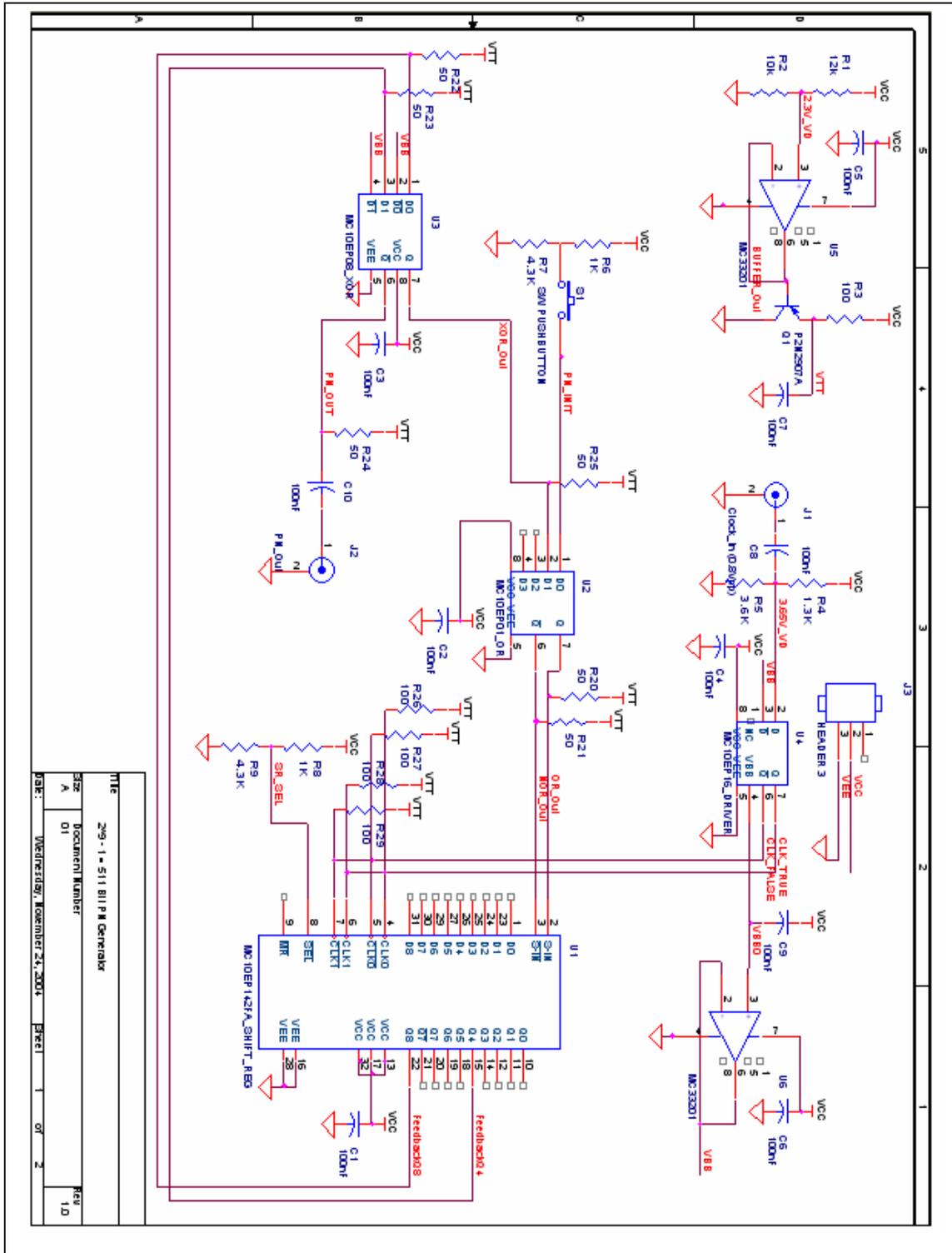
a velocity of propagation of 194.6×10^6 m/s. Thus, using the tenth of a wavelength rule of thumb for transmission lines, at any frequency beyond 350 MHz, impedance mismatches would begin to affect the performance of the PN generator.

The next generation of the PN generator must have 50-ohm traces to push the maximum clock frequency up to one Gigahertz. Additionally, the next generation board will use two 9-bit shift registers to generate a PN sequence of length $2^{18} - 1 = 292,143$ bits. This longer sequence will drastically improve the dynamic range of the channel sounder.

References

- [1] Anderson, Christopher R. "Design and Implementation of an Ultrabroadband Millimeter-Wavelength Vector Sliding Correlator Channel Sounder and In-Building Multipath Measurements at 2.5 & 60 GHz". [Online Document], 2002 May 6, [cited 2005 May 19], Available HTTP: <http://scholar.lib.vt.edu/theses/available/etd-05092002-101656/>
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Appendix A: PN Generator Schematic



Title	
299 - 1 - 511 B11 PN Generator	
Size	
A	Document Number
01	
Date	
01/27/2004	Version
1	of
2	Rev
1.0	